DFT-based Synchrophasor Estimation Algorithms and their Integration in Advanced Phasor Measurement Units for the Real-time Monitoring of Active Distribution Networks

THÈSE N^{O} 6906 (2016)

PRÉSENTÉE LE 5 FÉVRIER 2016

À LA FACULTÉ DES SCIENCES ET TECHNIQUES DE L'INGÉNIEUR
LABORATOIRE DES SYSTÈMES ÉLECTRIQUES DISTRIBUÉS - CHAIRE EOS HOLDING
PROGRAMME DOCTORAL EN ENERGIE

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES

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Suisse
2016

And in the end
the love you take
is equal to the love you make.

A mia nonna Marisa,
a mio zio Alfredo

Acknowledgements

Few but sincere words for those people who came along with me during this four years-long journey that looks like it started yesterday.
First of all, I would like to express my heartfelt gratitude to Mario, a competent and intimate supervisor, almost a friend, that has given me the opportunity to start this experience. I am really grateful for the trust you put in me and the responsibilities you gave me that have allowed my personal and professional growth in a particularly friendly environment.
Next a big thanks to my colleagues of DESL-PWRS group and particularly to Asja, Fabrizio, Lorenzo and Marco with whom I have spent most of my time, inside and outside the lab, during the last four years. Friends rather than colleagues!
Thanks to my parents that supported me from the moment I took the decision to move abroad.
Last but not least, a sincere thanks to Rita, who decided to join me in this adventure. I love you!

Poche ma sentite parole per tutte quelle persone che mi hanno accompagnato in questo viaggio di quatto anni che sembra essere iniziato ieri.
Prima di tutto un grazie di cuore a Mario, un relatore competente e vicino, quasi un amico, che mi ha datto l'opportunità di intraprendere questa esperienza. Sono davvero grato per la fiducia riposta in me e per le responsabilità affidatemi che mi hanno permesso di crescere umanamente e professionalemnte in un ambiente particolarmente sereno.
Un grande grazie a tutti i miei colleghi del gruppo DESL-PWRS ed in particolare ad Asja, Fabrizio, Lorenzo e Marco con cui ho passato la maggior parte del mio tempo, dentro e fuori dal laboratorio, durante gli ultimi quattro anni. Amici più che colleghi!
Un grazie va ai miei genitori che mi hanno sostenuto fin dal momento in cui ho preso la decisione di spostarmi all'estero.
Infine, un grazie sincero a Rita, che ha deciso di seguirmi in questa avventura. Ti amo!

Lausanne, 9 November 2015 Paolo

Abstract

The increasing penetration of Distributed Energy Resources (DERs) at the low and medium-voltage levels is determining major changes in the operational procedures of distribution networks (DNs) that are evolving from passive to active power grids. Such evolution is causing non-negligible problems to DN operators (DNOs) and calls for advanced monitoring infrastructures composed by distributed sensing devices capable of monitoring voltage and current variations in real-time.

In this respect, Phasor Measurement Units (PMUs) definitely represent one of the most promising technologies. Their higher accuracy and reporting rates compared to standard monitoring devices, together with the possibility of reporting time-tagged measurements of voltage and current phasors, enable the possibility to obtain frequent and accurate snapshots of the status of the monitored grid. Nevertheless, the applicability of such technology to DNs has not been demonstrated yet since PMUs where originally conceived for transmission network applications.

Within this context, this thesis first discusses and derives the requirements for PMUs expected to operate at power distribution level. This study is carried out by analyzing typical operating conditions of Active Distribution Networks (ADNs). Then, based on these considerations, an advanced synchrophasor estimation algorithm capable of matching the accuracy requirements of ADNs is formulated. The algorithm, called iterative-interpolated DFT (i-IpDFT) improves the performances of the Interpolated-DFT (IpDFT) method by iteratively compensating the effects of the spectral interference produced by the negative image of the spectrum and at the same time allows to reduce the window length up to two periods of a signal at the nominal frequency of the power system.

In order to demonstrate the low computational complexity of such an approach, the developed algorithm has been subsequently optimized to be deployed into a dedicated FPGA-based PMU prototype. The influence of the PMU hardware components and particularly the effects of the stability and reliability of the adopted UTC-time synchronization technology have been verified.

The PMU prototype has been metrologically characterized with respect to the previously defined operating conditions of ADNs using a dedicated PMU calibrator developed in collaboration with the Swiss Federal Institute of Metrology (METAS). The experimental validation has verified the PMU compliance with the class-P requirements defined in the IEEE Std. C37.118 and with most of the accuracy requirements defined for class-M PMUs with the exception of out of band interference tests.

Acknowledgements

Keywords: synchrophasor, Phasor Measurement Unit, Active Distribution Network, Discrete Fourier Transform, Interpolated DFT, Modulated Sliding DFT, Field Programmable Gate Array, Global Positioning System, calibration, IEEE Std. C37.118.

Résumé

L'accroissement de la pénétration des ressources énergétiques distribuées aux niveaux basse et moyenne tension dans les réseaux de distribution de l'énergie électrique a conduit à leur évolution en réseaux de distribution actifs. Ce changement est à l'origine de différents problèmes rencontrés par les opérateurs de réseaux de distribution, résultant du manque d'infrastructure de surveillance capables de contrôler les variations de tension et de courant en temps réel.
À cet égard, les "Phasor Measurement Units" (PMUs) représentent certainement l'une des technologies les plus prometteuses. Leur précision et fréquence d'échantillonnage élevée par rapport aux dispositifs de surveillance classiques, ainsi que la possibilité d'associer un horodatage aux mesures des phaseurs de tension et de courant, permettent d'obtenir des mesures plus précises de l'état du réseau surveillé. Toutefois, l'application de cette technologie au réseaux de distribution n'a pas encore été démontrée, puisque les PMUs étaient conçus à l'origine pour des applications dans les réseaux de transmission.
Dans ce contexte, en premier lieu cette thèse discute et identifie les exigences minimales de précision pour des PMUs conçus pour une utilisation au niveau des réseaux de distribution. Cette étude a été réalisée par l'analyse des conditions typiques de fonctionnement des réseaux de distribution. Puis, sur la base de ces considérations, un algorithme pour l'estimation de synchrophaseur capable de satisfaire les exigences précités a été formulée. L'algorithme, appelé "iterative-Interpolated DFT" (i-IpDFT), améliore les performances de la technique "Interpolated DFT" (IpDFT) en compensant de manière itérative les effets de l'interférence spectrale produite par l'image négative du spectre et, en même temps, permet de réduire la longueur de la fenêtre jusqu'à deux périodes d'un signal à la fréquence nominale du système de puissance.
Afin de démontrer la faisabilité d'une telle approche, l'algorithme développé a ensuite été optimisé pour être déployé au sein d'un prototype de PMU implanté sur une plateforme FPGA. L'influence des composants du prototype et en particulier les effets de la stabilité et la fiabilité de la technologie de synchronisation au temps UTC, ont été vérifiées.
Le prototype du PMU a été caractérisée métrologiquement par rapport aux conditions d'exploitation définies précédemment, en utilisant un calibreur pour PMUs développé en collaboration avec l'Institut Fédéral de Métrologie Suisse (METAS). La validation expérimentale a démontrée la conformité du PMU développée avec les dispositions définies par la norme IEEE C37.118 pour la class-P et avec la plupart des dispositions définies pour la classe-M, à l'exception des tests "out of band interference".

Mots clefs : synchrophasor, Phasor Measurement Unit, Réseau de Distribution Actif, Transformation de Fourier Discrète, DFT interpolé, Modulated Sliding DFT, Field Programmable Gate Array, Global Positioning System, calibration, IEEE Std. C37.118.

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Introduction

Motivation of the Thesis

The power distribution infrastructure has recently been undergoing a substantial evolution due to the increasing penetration of Distributed Energy Resources (DERs) at the low and medium-voltage levels. In particular, during the last decade, the intensive deployment of renewable energy resources (RERs) into the power distribution grid has considerably reshaped this level of the electrical infrastructure. The term Active Distribution Networks (ADNs) has emerged to define power distribution grids that [9, 10]:

> [...] have systems in place to control a combination of distributed energy resources, defined as generators, loads and storage. Distribution system operators (DSOs) have the possibility of managing the electricity flows using a flexible network topology. DERs take some degree of responsibility for system support, which will depend on a suitable regulatory environment and connection agreement.

Such an evolution is causing non-negligible changes in the operational practices of DN operators (DNOs) that can no longer assume the passivity of their electrical grids and have to face increasing challenges introduced by the high volatility of the RERs. In particular such a change has resulted in:

- frequent violations of operational constraints (e.g.,voltage limits and line ampacities);
- higher and non-predictable dynamics compared to transmission networks (e.g., transitions from grid-connected to islanded operations [11]);
- incorrect detection of power-system faults;
- limited amount of grid controlled resources.

As a consequence, DNOs can no longer manage their infrastructure with traditional and consolidated approaches and are standing in front of a crossroad. The first option is to invest in grid reinforcement. Such a choice would involve a non negligible increase of CAPEX and, if not properly planned, might not represent the optimal solution in the long-term. Additionally

grid reinforcement does not imply the control of the flexible resources available in ADNs.
The second option refers to the introduction of a high-performance monitoring infrastructure that could leverage the availability of distributed sensing devices to monitor, in real-time, the ADN state. Such an infrastructure, besides considerably reducing the required investments compared to grid reinforcement, might serve as a backbone for a series of power system functionalities that are usually embedded into any Energy Management System (EMS). These include [12, 13, 14]:

- optimal voltage/congestion control;
- updated protection schemes;
- local load balance;
- losses minimization.

Nevertheless, it is worth pointing out that standard EMS refresh rates are usually in the order of few seconds, values that are not sufficient to monitor and control in real-time ADNs. As already mentioned, the higher volatility of ADN DERs calls for refresh rates of the above-listed applications that are in the order few hundred of milliseconds for fault management applications and few seconds for most of control applications. Additionally, typical accuracies and latencies of current EMSs, which have been mainly designed around the availability of Remote Terminal Units (RTUs) data, might not satisfy the requirements of the above mentioned applications.
Within this context, Phasor Measurement Units (PMUs) definitely represent one of the most promising technologies to revamp the EMS architectures. Their higher accuracy and reporting rates, compared to RTUs, match the higher variability and volatility of DERs hosted in ADNs. Additionally, the possibility of reporting time-tagged measurements of voltage and current phasors, enables the possibility to obtain time-coherent snapshots of the monitored grid with a consequent improvement of the EMS control functions.
Nevertheless, the applicability of such technology to DNs has not been demonstrated yet at power distribution level, as PMUs where originally conceived for transmission network applications. In particular their actual accuracy levels seem insufficient to correctly monitor ADN voltage and current variations.
In this context, the thesis, starting from the definition of the accuracy requirements needed by PMUs expected to operate at power distribution level, aims at defining a novel synchrophasor estimation (SE) algorithm that is capable of matching these operating conditions. The integration of the proposed algorithm in an FPGA-based PMU prototype is then presented and validated by means of a metrological characterization of the PMU performances.

Organization of the Thesis

The thesis is organized as follows.
Chapter 1 introduces the nomenclature related to synchrophasors that is used in the thesis.

Then, it addresses the problem of time-synchronization for the case of PMUs and lists the available time dissemination technologies and methodologies to metrologically assess their performances. The PMU compliance verification according to the IEEE Std. C37.118 [1, 8] is also presented and properly analyzed with respect to the proposed metrics and testing conditions. Finally the Chapter presents a scientific literature review mainly focused on the available synchrophasor estimation techniques, associated PMU prototypes and their metrological characterization.
In Chapter 2 the PMU accuracy requirements for their application to ADN monitoring are first derived by analyzing the typical operating conditions of this kind of power systems. In particular, the derivation of the steady-state requirements is mainly based on simulation results aimed at evaluating typical magnitude and phase angle differences between voltage and current phasors at the extremities of a transmission line with typical parameters of medium voltage cables and overhead lines. Finally, the requirements with respect to signal distortion and power system dynamics are briefly discussed based on the most up-to-date official literature in the field of power quality [15].
Based on these considerations, an advanced synchrophasor estimation (SE) algorithm capable of matching the accuracy requirements of ADNs and being deployed in a relatively cheap PMU prototype, is formulated in Chapter 3. The algorithm represents a considerable improvement with respect to typical accuracies of classical Interpolated-DFT (IpDFT) SE techniques and at the same time allows to reduce the window length up to 2 periods of a signal at a nominal frequency of the power system. The algorithm is based on the iterative compensation of the spectral interference produced by the negative image of the spectrum and it is derived starting from fundamental concepts related to the Discrete Fourier Transform theory, like aliasing and spectral leakage. The Chapter also contains some considerations on the optimal choice of the DFT parameters when applying such a technique to synchrophasor estimation and a dedicated Section that reviews the most common and efficient techniques to calculate the DFT in real-time. Finally, the proposed SE algorithm, called *iterative-Interpolated DFT* (i-IpDFT) is formulated and presented together with numerical simulation results aimed at quantifying the improvement brought by such a technique.
Chapter 4 presents the integration of such a SE algorithm into an FPGA-based PMU prototype and is meant to demonstrate the low computational complexity of the proposed i-IpDFT technique. The adopted hardware platform is first presented in terms of its main hardware components. Then, the FPGA design and resources allocation are described with a particular focus on the deployment of the proposed SE algorithm on such an hardware platform. Next, the synchronization of the SE process to an UTC-time reference provided by a stationary GPS receiver is discussed and the effects of the stability and reliability of the adopted synchronization technology verified. The Chapter is concluded with few remarks on the resources allocation of a dual-core CPU that is mainly dedicated to the synchrophasor data streaming and PMU remote configuration.
Chapter 5 presents the metrological characterization of the developed PMU prototype. The performance assessment has been carried out using a dedicated PMU calibrator, developed in collaboration with the Swiss Federal Institute of Metrology (METAS), designed to metrologi-

cally characterize the performances of PMUs that will operate in ADNs. As demonstrated in Chapter 2, these measurement devices, and therefore the related calibration systems, must be characterized by higher accuracies compared to state-of-the-art devices. In this respect, the Chapter lists the main hardware components of the developed PMU calibrator together with a procedure to metrologically characterize them. Next, the experimental verification of the IEEE Std. C37.118 compliance is presented with respect to both steady-state and dynamic tests. The final Section of the Chapter presents a further experimental verification of the PMU performances with signals that emulates typical operating conditions of ADNs.
Finally, the last Chapter concludes the thesis with a summary of the main outcomes and remarks.

Original Contributions of the Thesis

The original contributions included in this thesis are summarized here below:

- A method to quantify the accuracy requirements of PMUs that are expected to operate in ADNs. This is based on dedicated simulations aimed at representing typical ADN operating conditions. Due to the high amount of power-system applications that can exploit the availability of PMU at such a voltage level, the analysis has focused on ADNs monitoring. To the best of the author's knowledge such analysis represents a first attempt towards the definition of the accuracy requirements that PMUs must satisfy to correctly operate in ADNs. The developed software also represents a generic approach to verify if a specific PMU technology can be used to properly monitor an electrical grid subject to specific operating conditions. The simulation results have also verified the inadequacy of the IEEE Std. C37.118 [1], and particular its 1% TVE limit, when applied to the design and testing of PMUs operating in ADNs.
- A novel SE algorithm, called iterative-Interpolated DFT (i-IpDFT) that represents a considerable improvement with respect to classical Interpolated-DFT (IpDFT) synchrophasor estimation techniques in terms of both accuracies and response times, as it allows reducing the window length up to 2 periods of a signal at the nominal frequency of the power system without compromising the estimation uncertainty. The SE algorithm performances have been verified by dedicated simulations that have demonstrated the considerable improvements brought by such a technique with respect to the typical performances of classical IpDFT methods.
- The integration of the i-IpDFT algorithm in a PMU prototype based on a Xilinx Zynq System-on-Chip (SoC), a hardware platform that combines the flexibility of a real-time processor with the high-speed and intrinsic determinism of a Field Programmable Gate Array (FPGA). The thesis has illustrated the non-trivial aspects related to the deployment of the proposed i-IpDFT synchrophasor estimation algorithm into such an embedded platform, with a particular focus on the synchronization of the developed PMU prototype to the UTC-time reference provided by the GPS.

- A novel calibrator for PMUs expected to operate in ADNs, developed in collaboration with the Swiss Federal Institute of Metrology (METAS). The calibrator is based on a National Instrument PXI system and designed to match the higher accuracy requirements needed by PMUs operating in ADNs. In this respect every hardware component within the calibration chain has been metrologically characterized. This has allowed to achieve an overall accuracy of the calibrator in the order of 0.01% TVE during steady-state conditions.

- The experimental validation of the metrological performances of the developed PMU prototype that has proven to be compliant with the IEEE Std. C37.118 [1] specifications. In particular, the developed PMU prototype has demonstrated to be compliant with the class-P requirements defined in [1] and pass every test designed for class-M PMUs with the exception of the Out-of-band interference test. The PMU has also been tested against specific testing conditions, not included in the IEEE Std. [1], designed to verify PMU compliance with typical operating conditions and signal distortions characterizing ADNs.

1 Definitions and State of the Art

This chapter first defines the basic concepts and terminology that will be used later along this thesis, related to Phasor Measurement Units and their synchronization. Then, it analyzes the only available standard in the field of Phasor Measurement Units, namely the IEEE Std. C37.118, and particularly the proposed PMU compliance procedure. Finally, in order to help the reader in delineating the context where the thesis is positioned, it reviews the scientific literature in the context of synchrophasor estimation and in the development of dedicated PMU hardware architectures.

1.1 Definitions

This section, starting from the adopted signal model, recalls the theoretical definition of a *phasor* and derives the concepts of *synchrophasor*. Then, it illustrates the basic architecture of a generic Phasor Measurement Unit together with a preliminary analysis of its components and the available time-synchronization technologies. It is worth noting that this section, while being in agreement with what defined in the reference IEEE Std. C37.118.1-2011 [1], aims at clarifying some aspects that are still ambiguous in this Standard itself and tries to answer some open questions.

1.1.1 Signal Model

Electrical power is traditionally delivered from the generators to the end-users through an infrastructure that is mainly composed by AC power systems. As a consequence, during normal operating conditions of the power system, voltage and current waveforms are usually modeled as signals characterized by a single sinusoidal component with constant parameters:

$$x(t) = A_0 \cdot \cos\left(2\pi f_0 t + \varphi_0\right) \tag{1.1}$$

being A_0 the nominal peak-amplitude, φ_0 the initial phase (i.e. for $t = 0$) and f_0 the nominal frequency of the power system (i.e. 50 or 60 Hz).
However, even if in normal operating conditions, a power system is never in a steady state. As a consequence the parameters of (1.1) are rarely time-invariant and typically exhibit various dynamic behaviors. Frequency fluctuations are definitely the most evident phenomena and are typically related to changes in load/generation imbalances and to the interactions between real power demand in the grid, inertia of large generators and the operation of automatic speed controls with which most generators are equipped [4]. Additionally, when faults or other switching events take place, those variations can involve even larger frequency fluctuations [11].
Similarly, the waveform amplitude and phase are also affected by transient phenomena. Those can be relatively slow like in the case power swings (i.e. amplitude and phase oscillations typically characterized by frequencies in the range of 0.1-10 Hz) or faster like in the case of switching events or faults that usually produce step changes in the voltage and current waveforms, with spectral components that can even reach several hundreds of kilohertz.
Additionally, the main tone is often corrupted by other superposed signals that can be of different natures. In the literature the following interfering signals are usually considered:

- *Harmonics*, namely spectral components at frequencies that are integer multiples of the AC system instantaneous frequency that, as reminded previously, can be different from the nominal one f_0. These signals are typically produced by power electronics devices: in transmission systems these can be Flexible AC Transmission Systems (FACTS) or HVDC connections. On the other hand, at distribution level most of the harmonics are generated by converters that are typically interfacing distributed generation units or non-linear loads [4]. The literature on PMUs usually considers the effects of harmonics up to the 50^{th}, assuming that higher frequency components are either attenuated by the analog front-end filters of the PMU or too far in the frequency spectrum to be considered relevant.

- *Inter-* and *sub-harmonics*, namely spectral components at frequencies that are not integer multiples of the system frequency: inter-harmonics are characterized by a frequency that is bigger than the nominal one f_0 and sub-harmonics by a frequency that is smaller than f_0. The causes of inter- and sub-harmonics are usually static frequency converters, cycloconverters, subsynchronous converter cascades, induction motors, arc furnaces and all loads not pulsating synchronously with the fundamental power system frequency [16].

- aperiodic components like *decaying DC offsets* that are likely to appear during power system transients (consider, for instance, the case of a decaying short-circuit current or inrush of transformers/induction motors). The involved time constants can vary in the range between 0.1 and 10 s.

- *wide-band noise* that includes both the “measurement noise” (namely the noise added by any measurement equipment) and the so-called “grid noise”; regarding the latter

term, the most well known phenomena are the thermal noise (also known as Johnson–Nyquist noise), the corona effect and the partial discharges. Both sources are usually modeled as a zero-mean Gaussian noise processes.

As a consequence, a generalized and more complete signal model that takes into account each one of the above mentioned dynamics and interfering signals can be derived:

$$x(t) = A(t) \cdot \cos\left(2\pi f(t)\, t + \varphi_0\right) + \sum_{h=1}^{H} A_h(t) \cos\left(2\pi f_h(t)\, t + \varphi_h\right) + A_{DC}(t) e^{-\frac{t}{\tau}} + \epsilon(t) \qquad (1.2)$$

where:

- The first term represents the main tone of the spectrum, characterized by an instantaneous frequency $f(t)$ that is typically very close to the nominal frequency of the power system f_0 (50 or 60 Hz depending on the region), an instantaneous peak amplitude $A(t)$, and an instantaneous phase $\psi(t) = 2\pi f(t)\, t + \varphi_0$. The assumption of having a constant initial phase φ_0 is both mathematically and physically correct. It implies that the instantaneous phase variations are only due to the generators frequency variations and it avoids the possibility of having multiple couples of frequency and initial phase that produce the same $\psi(t)$.

- The second term models the contribution of any superposed sinusoidal tone excluding the main one, namely it includes all the effects of harmonics, inter- and sub-harmonics. Each one of the tones is characterized by an instantaneous frequency $f_h(t)$, peak amplitude $A_h(t)$ and instantaneous phase $\psi_h = 2\pi f_h(t)\, t + \varphi_h$, being φ_h the initial phase. In normal operating conditions the peak amplitude must be at least one order of magnitude lower than the one of the main tone $A(t)$, but no hypothesis can be made with respect to the instantaneous phase that does not necessarily have to match the one of the main tone.

- The third term models a decaying DC component characterized by an initial amplitude A_{DC} and an arbitrary time-constant τ.

- The last element represents a wide-band noise that includes any other contribution not considered with the previous terms.

1.1.2 Phasor

The phasor transformation has been historically adopted in electrical engineering to simplify the analysis of electrical systems in sinusoidal steady state. It consists in a one-to-one mapping between time-harmonic functions and complex numbers that can be adopted if and only if the instantaneous frequency f, peak amplitude A and initial phase φ are *time-invariant*, namely if and only if the sinusoidal signal $x(t)$ is *stationary*. In particular, such a transformation allows

to represent a sinusoidal function of time like the one expressed by equation (1.1) with a single complex constant and vice versa. In order to derive it, we can rewrite equation (1.1) as:

$$x(t) = A \cdot \cos\left(2\pi f t + \varphi\right) \tag{1.3}$$
$$= \mathrm{Re}\left\{A \cdot e^{j(2\pi f t + \varphi)}\right\} \tag{1.4}$$
$$= \mathrm{Re}\left\{A \cdot e^{j\psi(t)}\right\} \tag{1.5}$$

where the dependency of $\psi(t)$ on time can be disregarded due to the stationarity of $x(t)$. We can then associate to the sinusoid $x(t)$ the complex number X and call it *phasor*:

$$x(t) \rightleftarrows X \triangleq A \cdot e^{j\psi} \tag{1.6}$$
$$= A \cdot \left[\cos(\psi) + j\sin(\psi)\right] \tag{1.7}$$
$$= X_r + jX_i \tag{1.8}$$

where the subscript r and i identify the real and imaginary parts of X. A phasor can be represented either in polar (1.6) or rectangular (1.8) coordinates and the transformation from one set of coordinates to the other can be done using the well-known Euler identity (1.7).

1.1.3 Synchrophasor

The phasor concept cannot be directly applied to the analysis of a real AC power system for the simple reason that the *stationarity hypothesis* does not hold in the real world. Nevertheless, even when the power system is not in steady-state (e.g. during electromechanical oscillations, power swings, etc.), the voltage and current variations can be assumed relatively slow and be treated as a series of steady-state conditions where the stationarity hypothesis holds (*quasi steady-state* approximation) and the phasor analysis can be still applied.
Still, without the hypothesis of sinusoidal steady-state, it is impossible to compare phasor measurements along different locations in a grid without a common time reference (i.e., common phase reference). This is due to the fact that the value of the instantaneous phase $\psi(t) = 2\pi f t + \varphi$ is intrinsically depending on the time scale t and, consequently, the phase of a sinusoid cannot be univocally defined unless referenced to a common time reference.
For this reason the phasor concept has been extended to the *synchrophasor* one that has been first defined in the IEEE Std. 1344-1995 [17] as:

> [...] a phasor calculated from data samples using a *standard time signal as the reference for the sampling process*. In this case, the phasors from remote sites have a *defined common phase relationship*. [...]

Thanks to the explicit reference to a common time-reference t, the synchrophasor concept allows to define a common phase relationship between phasors from remote sites. Additionally, it is not restricted to the analysis of stationary systems since a synchrophasor can be associated

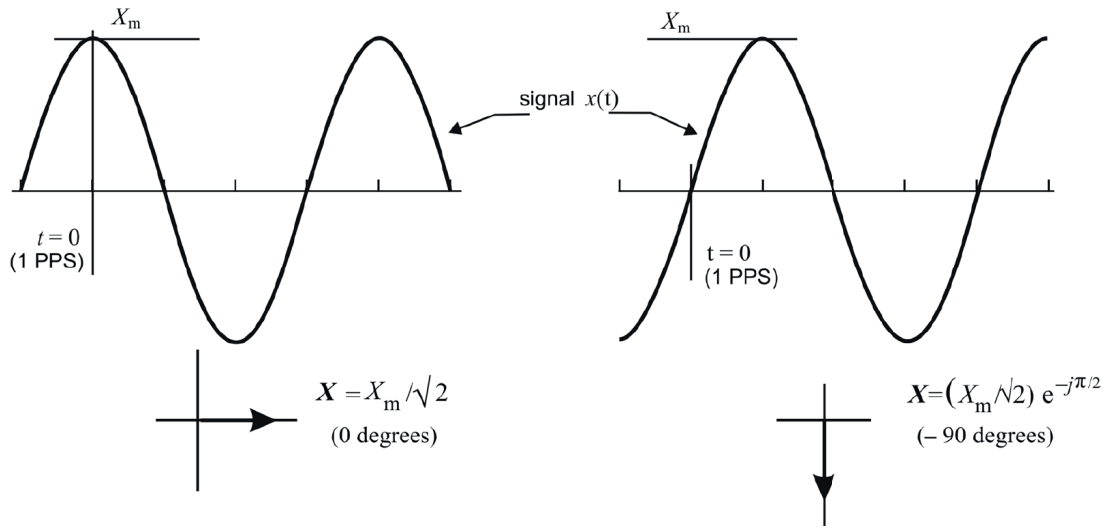


Figure 1.1 – The phase convention for synchrophasors, adapted from [1], for a signal of amplitude X_m.

to any waveform characterized by a dominant sinusoidal component, also, during power system transients and with superposed interfering signals[1].
The synchrophasor concept, and particularly the analytical definition of its phase, has been reviewed later in the IEEE Std. C37.118.1-2011 [1] and defined as:

> [...] the instantaneous phase angle relative to a cosine function at the nominal system frequency synchronized to UTC. [...] Under this definition ψ is the offset from a cosine function at the nominal system frequency synchronized to UTC. [...]

The above IEEE Std. definition, which refers the phase to an hypothetical signal at the nominal frequency f_0 synchronized to the Coordinated Universal Time (UTC), is restrictive and might generate ambiguities. A better and more generic definition of synchrophasor, can be given by referencing both amplitude and phase estimations to the same time reference. For this reasons the reminder of this thesis will use the following synchrophasor definition:

Definition. *The synchrophasor representation of the signal $x(t)$ in Equation (1.2) is the complex function $X(t)$ characterized by an instantaneous amplitude and phase corresponding to the instantaneous amplitude $A(t)$ and phase $\psi(t)$ of the main tone of $x(t)$ respectively, being t the UTC time-reference.*

As a consequence, in the case of the signal $x(t)$ represented in equation (1.2), the associated synchrophasor is:

$$x(t) \rightleftarrows X(t) \triangleq A(t) \cdot e^{j\psi(t)} \tag{1.9}$$

[1] It is worth pointing out that the synchrophasor refers only to the main tone of $x(t)$ and does not take into account any other contribution that might be present in the original signal.

$$= A(t) \cdot e^{j(2\pi f(t)t+\varphi)} \tag{1.10}$$

where $A(t)$ and $\psi(t)$ are the instantaneous peak-amplitude and phase of the main tone of $x(t)$ (see equation (1.2)).
As shown in Figure 1.1, such a convention implies that, if the sinusoidal waveform has its maximum at the UTC-second rollover (i.e. when the cosine has its maximum) the synchrophasor angle is 0 degrees. It is 90 degrees if the positive zero-crossing occurs at the UTC-second rollover.
According to the IEEE Std. C37.118, frequency is defined starting from the 1st order derivative of the instantaneous phase $\psi(t)$:

$$\frac{\mathrm{d}\psi(t)}{\mathrm{d}t} = \frac{\mathrm{d}}{\mathrm{d}t}\left[2\pi f(t)t + \varphi\right] \tag{1.11}$$

$$= 2\pi\left[f(t) + \frac{\mathrm{d}f}{\mathrm{d}t}t\right] \tag{1.12}$$

With the quasi steady-state assumption, the second term can be disregarded and frequency can be defined as:

$$f(t) = \frac{1}{2\pi}\frac{\mathrm{d}\psi(t)}{\mathrm{d}t} \tag{1.13}$$

Similarly, the Rate of Change of Frequency (ROCOF) is defined in the IEEE Std. C37.118 as the 1st order derivative of the frequency:

$$ROCOF(t) = \frac{\mathrm{d}f(t)}{\mathrm{d}t} \tag{1.14}$$

It is worth underlying that the definitions given in equations (1.13) and (1.14) disagree as equation (1.13) has been obtained with an approximation ($\mathrm{d}f/\mathrm{d}t = 0$) that would lead to $ROCOF = 0$.

1.1.4 Phasor Measurement Unit

According to the IEEE Std. C37.118.1-2011 [1], a Phasor Measurement Unit (PMU) is a device that provides an estimate of the synchrophasors, frequency and ROCOF of the acquired voltage and/or current waveforms, based on a common UTC time reference.
Typically a PMU is installed into an electrical substation and interfaced to the electrical grid via standard instrument transformers (see Figure 1.2), namely voltage and current transformers that transform the power system voltage and current waveforms to levels appropriate for the PMU analog front-end. Several instrument technologies can be used and they are partially reviewed in [2].
The logic architecture of a generic PMU is shown in Figure 1.3. The PMU, in order to report synchronized measurement, needs to be equipped with a time-synchronization module capable of receiving the UTC absolute time from a reliable and accurate time-source (see

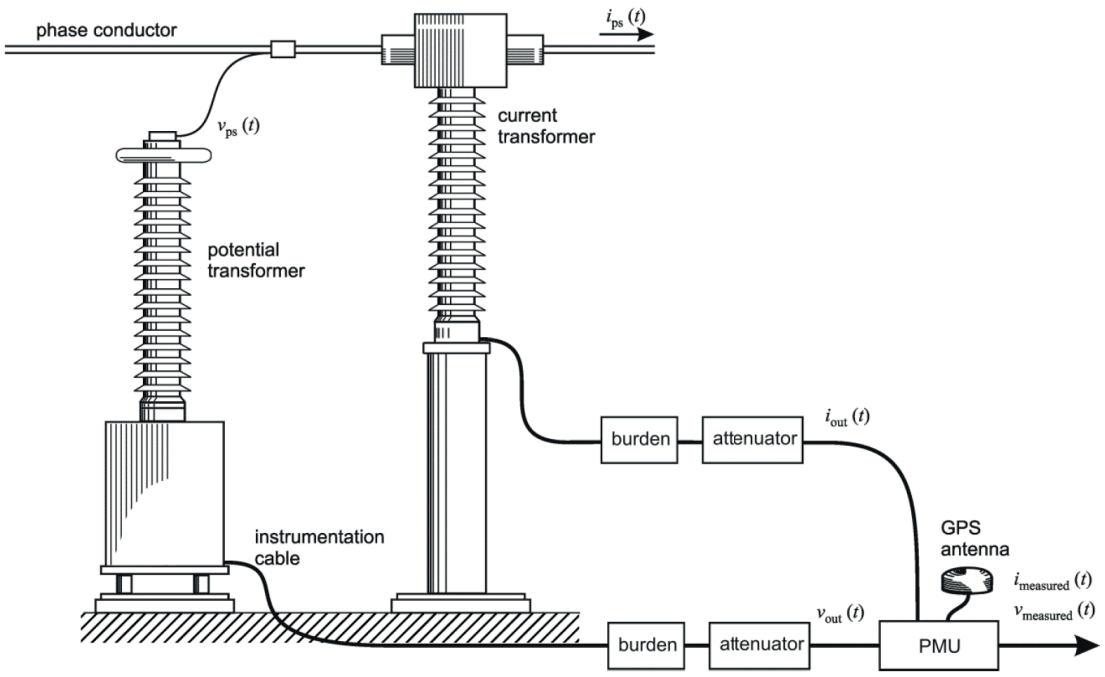


Figure 1.2 – Typical electrical substation setup to interface a PMU to the electrical grid (adapted from [2]).

Section 1.2 for further details on the PMU synchronization). The time-sync unit internally generates the "time-base" namely a stable and accurate internal time reference that is used by the signal conditioning and A/D conversion unit to discipline[2] the sampling process of the input waveforms (as many as the number of connected input channels). The sampled waveforms are then transferred, sample by sample, to the Synchrophasor Estimation (SE) algorithm, usually the most computationally expensive logic unit of a PMU that extracts the main tone parameters using any of the techniques described in literature. The estimated values are then transferred to the data encapsulation and streaming unit that encapsulates and streams the data according to the IEEE Std. C37.118.2-2011 [18] data-transmission protocol.

It might be obvious, but still worth pointing out that each one of the logical components highlighted in Figure 1.3 contributes to the global uncertainty that intrinsically characterizes the PMU estimations of amplitude, phase, frequency and ROCOFs. In particular:

- The time-sync unit, depending on the adopted time source and dissemination technology, might deteriorate the synchronism of the sampling process (i.e., its alignment to the UTC-second rollover and the accuracy of the sampling time). Such an uncertainty can have non-negligible effects on the overall measurement accuracy, particularly in

[2]Such a functionality is quite common in PMUs but not mandatory. The synchronization of the sampling process to a common time-reference can be also achieved by post processing the acquired samples

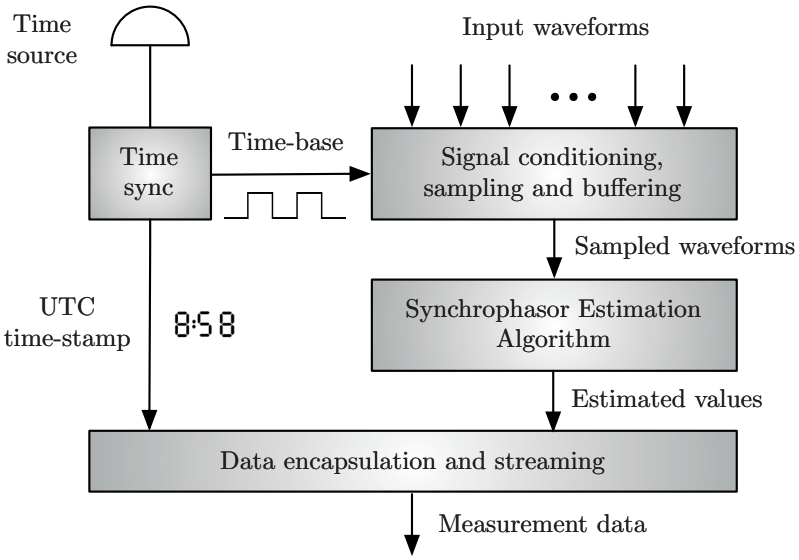


Figure 1.3 – Block scheme of a generic Phasor Measurement Unit.

the estimation of the phase[3].

- The signal conditioning and sampling unit intrinsically introduces an uncertainty that is mainly related to: the intrinsic noise, eventual non-linearities and gain errors introduced by the analog filtering stage (anti-aliasing filters for instance); the quantization error introduced by the A/D converters, even though it can be typically neglected if at least 14-bits A/D converters are employed.

- The synchrophasor estimation algorithm is characterized by its own accuracy levels that are typically assessed in a simulation environment following the guidelines given by the IEEE Std. C37.118 [1]. Nevertheless, these simulation environments cannot take into account every possible power system operating conditions and the SE algorithm estimations might be biased when processing non-contemplated waveforms. For instance, it has already been demonstrated that different SE algorithms might produce different estimations, particularly when exposed to power system transients [19].

Additionally, although this aspect will not be treated along this thesis, it should not be forgotten that a PMU must be interfaced to the high voltage/current signal through dedicated instrument transformers (see Figure 1.2) that are characterized by their own amplitude and phase uncertainties based on their specific accuracy class. For instance, in the case of standard magnetic core voltage and current transformers (VTs and CTs), their accuracy is generally limited to class 0.5%. This, according to the definition of the standards [20] and [21], translates, at full scale, to a maximum ratio error of 0.5% and a maximum phase error of 6 mrad for

[3]The time-sync uncertainty linearly translates in phase uncertainty based on the instantaneous frequency values following the formula $\Delta\psi = 2\pi f \Delta t$, being $\Delta\psi$ and Δt the phase and time uncertainties.

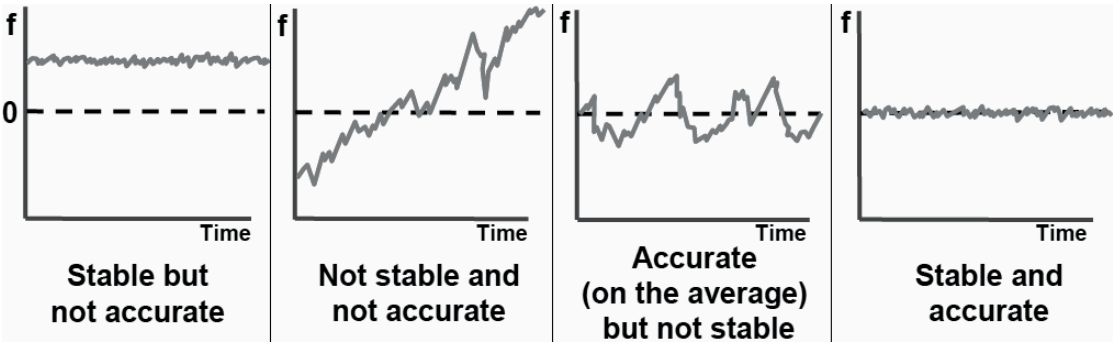


Figure 1.4 – Illustration of the stability and accuracy concepts.

VTs and 9 mrad for CTs. Such an uncertainty, in most of the cases, might exceed that of the connected PMU and deteriorate therefore the expected accuracies.

1.2 Absolute-time Synchronization

Synchrophasor measurements taken by PMUs shall be time-stamped with the UTC time corresponding to the time of measurement and therefore need to be synchronized to a UTC time reference. Such a characteristic differentiates this technology from any other power-system metering device. As a consequence the PMU performances are strictly correlated to the performances of the selected time-reference that must be carefully selected to achieve the desired accuracy levels and particularly to keep the Amplitude, Phase, Frequency and ROCOF Errors (see Section 1.3.3) within specific limits.

1.2.1 Accuracy and Stability of a Time-reference

A time-reference is an oscillator, namely an electronic circuit that produces a periodic, oscillating signal (typically sine or square wave) that might exhibit a variety of instabilities. These include aging, noise, and frequency changes with temperature, acceleration, ionizing radiation, power supply voltage, etc. The performances of an oscillator are usually expressed in terms of 2 parameters: its *accuracy* and its *stability* (see Figure 1.4). *Accuracy* is generally defined as the degree of conformity of a measured or calculated value to its definition and is related to the offset from an ideal value. In the case of oscillators the frequency offset, for

Table 1.1 – The stability of some of the most common oscillators, expressed as the value of the Allan deviation for an averaging period of 1 s (adapted from [7]).

Oscillator type	Quartz (TCXO)	Quartz (OCXO)	Rubidium	Commercial Cesium beam	Hydrogen Maser
Stability (@ 1 s)	1×10^{-8} to 1×10^{-9}	1×10^{-12}	5×10^{-11} to 5×10^{-12}	5×10^{-11} to 5×10^{-12}	1×10^{-12}

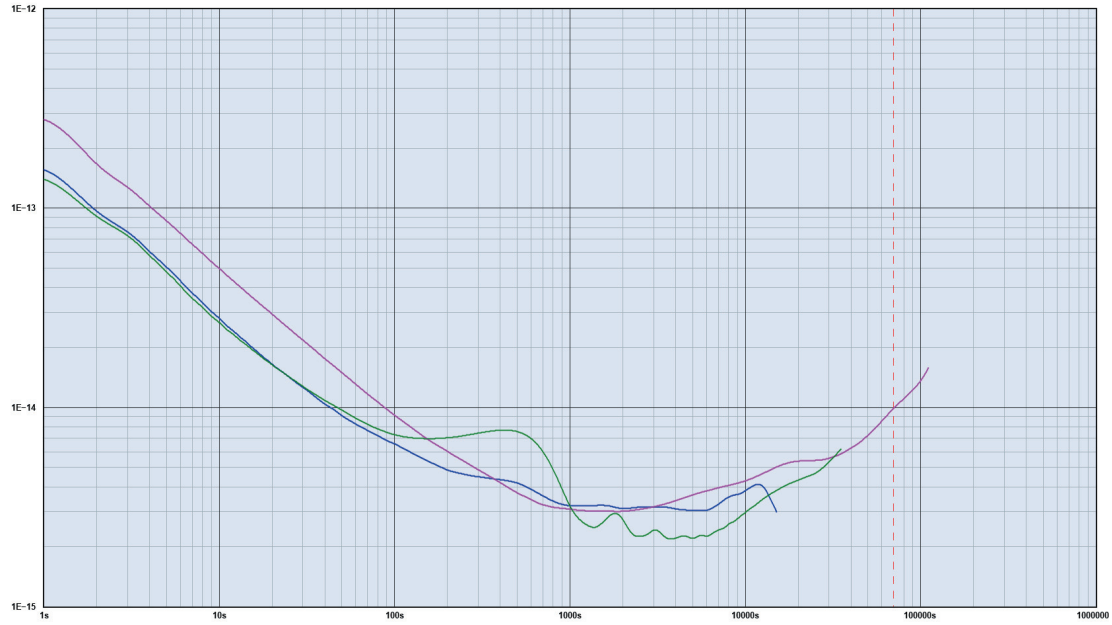


Figure 1.5 – Example of an Allan Deviation graph that shows the stability of three different Hydrogen MASERs increasing with higher averaging periods τ until they reach the so-called *noise floor*.

instance, is the difference between a measured frequency and an ideal frequency with zero uncertainty and can be measured by comparing the measurements to a reference oscillator. On the other hand, *stability* indicates how well an oscillator can produce the same time or frequency offset over a given time interval. In this respect Table 1.1 presents the stability characteristics of the most common oscillators.

The stability of an oscillator is usually expressed using the *Allan deviation*, a non-classical statistical estimate of the frequency or time fluctuations of a signal over a given time interval, also called averaging period (see [7] for further details). The Allan deviation can be calculated according to the following equation:

$$\sigma_y(\tau) = \sqrt{\frac{1}{2M-1}\sum_{i=1}^{M-1}(y_{i+1}-y_i)^2} \tag{1.15}$$

where y_i, $i = 1,\ldots,M$ is a set of M frequency offset measurements equally spaced in segments τ seconds long. Note that while standard deviation subtracts the mean from each measurement before squaring their summation, the Allan deviation subtracts the previous data point. This difference of successive data points removes the time dependent noise contributed by the frequency offset [22].

In this respect Figure 1.5 shows the Allan Deviations of 3 different MASERs. Their stability improves as the averaging period τ gets longer, since some noise types can be removed by averaging. At some point, however, more averaging no longer improves the results and this point is called the *noise floor* (it happens around the averaging period $\tau = 2000$ seconds).

Evidently, PMU performances are related to both accuracy and stability of their internal time-reference. Whereas the first can be easily achieved by an initial calibration of the oscillator and regular readjustments of its unavoidable drift, the latter identifies the reproducibility of the PMU estimates and therefore its inherent quality. As a consequence, stability is the most important parameter to be used when selecting a PMU time-base oscillator.

1.2.2 Time Dissemination Techniques

A time-reference can be either *internal* or *external*. Between them the latter is the preferred solution for PMUs and synchrophasor networks mainly because:

- it allows to synchronize multiple instruments without the need of replicating the time-source;
- depending on the intrinsic oscillator stability, internal time-sources need a continuous readjustment of their inherent drift. This is typically done using external and more stable time references;
- PMUs need absolute time information that cannot be synthesized internally but need to come from an external and certified UTC time-reference.

External time-sources need to be disseminated in order to be available for PMUs. This is an extremely delicate process that might deteriorate the quality of the time-reference. The main time dissemination technologies are the following:

Global Navigation Satellite Systems (GNSSs) In the PMU domain, the Global Positioning System (GPS) and generally speaking GNSSs are the most commonly adopted time-dissemination technologies for their good compromise between performances and costs. Other recognized GNSS systems are GLONASS and Galileo [23]. The satellites are typically located in the so-called medium earth orbit (MEO) and are equipped with accurate atomic clocks that derive the time information from a ground-based UTC-referenced primary clock. The dissemination is done using carrier signals over dedicated frequency channels: GPS, for instance, uses 2 dedicated frequencies, 1575.42 MHz (L1 signal) and 1227.60 MHz (L2 signal).

Network time transfer protocols Several protocols are available and can be used to synchronize clocks throughout a computer network: NTP (Network Time Protocol) [24] and PTP (precision Time Protocol) [25] are definitely the most well known. Unfortunately few of them guarantee the accuracy level requirements of PMUs. This is mainly due to the design and operation of the protocol itself, but also to the underlying physical medium that is used to disseminate the time and is usually shared with other users and applications. During the most recent years the PTP protocol and particular its version 2 [25] raised the interest of some PMU developer, mainly due to the increased accuracy

with respect to its predecessors. Still, the higher costs of such a time dissemination infrastructure (it should not be forgotten that the "network" needs to be deployed if not yet in place) do not attract many PMU developers and users. The hope is that with the coming version 3 (also known as "White rabbit" [26]) of the PTP the PMU accuracy can be cut down by, at least, two order of magnitudes.

Serial time codes They use a continuous stream of binary data to transmit information on date and time. The individual time code formats can be distinguished by the signal characteristics (e.g. modulated versus unmodulated signals), by the data rate, and by the kind of information included in the transmitted data. IRIG-B is definitely the most well known one and has been also suggested in [1] using the modified Manchester modulation for high-precision measurements.

Pulse Per Second (PPS) The synchronization using a train of pulses at a rate of one pulse per second (1 PPS) is a common feature of several scientific and industrial equipment. The rising edge of the pulse coincides with the second change but no absolute time information can be provided with such a technique that must be necessarily combined with other time dissemination systems.

1.2.3 Selection of the Time Reference

The following "figures of merit" are typically used when selecting among the different possible combination of time-sources and time dissemination technologies [2]:

- *Accuracy*: The degree of conformance between the measured synchronization signal and its true value.
- *Availability*: The capability of the synchronization system to provide usable timing services within the specified coverage area.
- *Continuity*: The probability that the synchronization system will be available for the duration of a phase of operation, presuming that the system was available at the beginning of that phase of operation.
- *Reliability*: The probability that a synchronization system will perform its function within defined performance limits for a specified period of time under given operating conditions.
- *Integrity*: The ability of the synchronization system to detect the timing signals' degradation and provide timely warnings to users.
- *Coverage*: The geographical area in which the application-specific synchronization system requirements for accuracy, availability, continuity, reliability, integrity, and coverage parameters are satisfied at the same time.

- *Ride-through capability*: The clock accuracy that is maintained and for how long upon loss of satellite synchronization.

According to this classification, GPS definitely represents the best time-dissemination technology for synchrophasor applications, due to its good compromise between performances and costs and to the relatively high availability and coverage.

1.3 The IEEE Std. C37.118 compliance

The only officially recognized PMU standard is the IEEE C37.118. Such a standard derives from a preliminary version of an IEEE Standard for synchrophasors, the IEEE Std. 1344-1995 [17], and has been first issued in 2005 [27], reviewed in 2011 [1, 18] and amended in 2014 [8]. It is composed by two parts: (i) Part I, the *IEEE Std. for Synchrophasor Measurements for Power Systems*, deals with the synchrophasor terminology and the synchrophasor measurement requirements and compliance verification; (ii) Part II, the *IEEE Standard for Synchrophasor Data Transfer for Power Systems*, mainly defines the synchrophasor message format, message types and communications.
The PMU compliance to the IEEE Std. is achieved by satisfying both the measurement requirements specified in [1] and amended in [8] and the communication requirements as described in [18]. Whereas the latter are straightforward to be accomplished, the former is a more challenging achievement as it involves several engineering competencies necessary to build a compliant PMU prototype. For this reason most of the IEEE Std. compliance verification involves test aiming at verifying the measurement compliance. To this purpose, [1] has defined a metrological procedure aimed at assessing the PMU accuracies during both steady state and dynamic conditions of a power system. This is done by defining specific tests and reference signals, aimed at artificially simulating various operating conditions of the electrical grid, together with the related compliance requirements. The PMU compliance is then assessed by comparing the PMU performances to the IEEE Std. requirements and verifying if they respect the previously defined limits.
In what follows the PMU compliance verification procedure proposed in [1] is summarized and commented. For further details the reader should make reference to what originally stated in the IEEE Standard [1], the related IEEE Guide [2] and the latest Test Suite Specification (TSS) [28].

1.3.1 Reporting Rates and Reporting Times

Synchrophasor measurements taken by PMUs must be reported regularly at a reporting rate F_r that is an integer number of times per second or an integer number of seconds per frame [1]. The reporting times shall be evenly spaced through each second, with the time of the first frame within the second coincident with the UTC second rollover (i.e., with a fractional second of 0).

According to the Standard [1] a PMU shall support the reporting rates 10, 25, 50 or 10,12, 15, 20, 30, 60 frames-per-second (fps) depending on whether the power system frequency f_0 is 50 or 60 Hz respectively. Higher reporting rates such as 100 or 120 frames-per-second are also encouraged in the Standard to support time-critical applications like power system protection and fault management. Nevertheless it is worth pointing out that only those PMU characterized by a shorter window length can afford to push their reporting rates up to these values, as the correlation between consecutive measurements can make such an increased information rate useless.

1.3.2 Performance Classes

PMUs shall be tested against the expected *operating conditions* and the targeted *power system applications*. With respect to the latter, the IEEE Std. [1] has defined two performance classes, corresponding to two distinct PMU applications and different compliance requirements:

- *P-class* is intended for Protection applications or any application requiring fast response times and reduced reporting latencies (see Section 1.3.3).
- *M-class* is intended for Measurement applications where more importance is given to the accuracy of the PMU estimations, and particularly to its capability to reject inter-harmonics, rather than their response times and reporting latencies.

It is worth noting that the performance classes defined in the IEEE Std. [1] do not discriminate between the use of PMUs in transmission or distribution networks and the various test types and compliance requirements have been derived by assuming the operating conditions of transmission networks. This is because PMUs have been originally deployed at such a level, mainly for the higher investment costs and the critical reliability of this infrastructure. As a consequence it is important to keep in mind that such a compliance verification might not be sufficient for a PMU that wants to operate at the power distribution level (see Chapter 2 for an analytical derivation of the accuracy requirements for PMUs operating in ADNs).

1.3.3 PMU Performance Evaluation

The evaluation of the PMU performances is typically performed by a dedicated PMU calibrator that is capable of characterizing the metrological characteristics of the PMU under test by comparing its estimations to a "true" value[4] and assessing its conformity to some predefined accuracy limits.
In this respect the metric to evaluate the PMU estimation errors together with those for the PMU response time and measurement reporting latency must be defined.

[4] Since the "true" value of a quantity is not something that can ever be known, in what follows the term "true" will be used to define a reference quantity characterized by a variance that is known and can be a priori considered much smaller that the one of the PMU estimation.

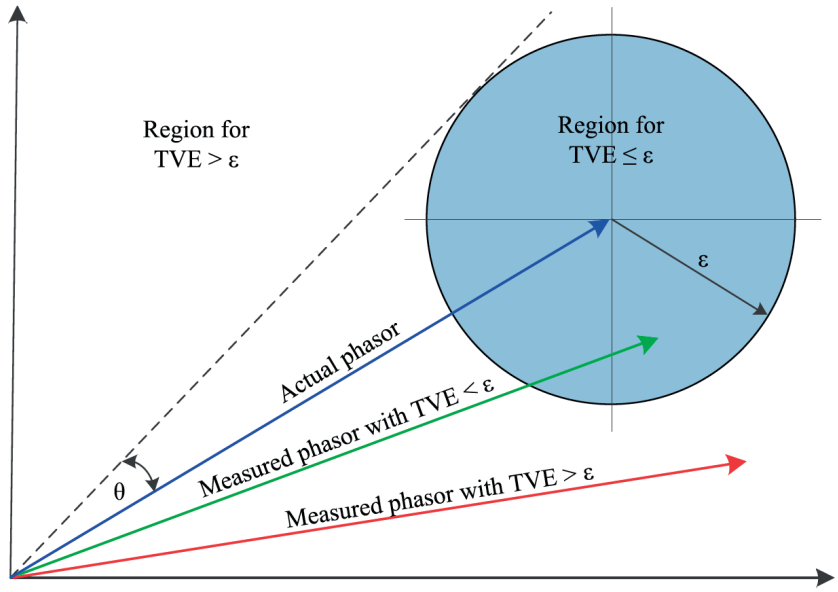


Figure 1.6 – Complex plane plot showing the "true" phasor in blue, the TVE circle centered around it, and two different phasor measurement that are compliant (in green) and not compliant (in red) with the TVE limit (adapted from [1]).

Total Vector Error

The PMU accuracy in estimating the true synchrophasor can be expressed independently in terms of the amplitude and phase errors or the real and imaginary part errors if rectangular coordinates are adopted. This is, for instance, the approach used in the case of instrument transformers, where the acceptable errors are expressed separately in terms of the allowed phase angle and magnitude error (see [29]).
Nevertheless sometimes it is useful to express the synchrophasor estimation error with a single value that includes both components. This quantity has been defined in [1] and is called *Total Vector Error* (TVE). The TVE is a real number that expresses the Euclidean distance between the true and estimated synchrophasors, normalized with respect to the amplitude of the true synchrophasor (see Figure 1.6):

$$TVE \triangleq \frac{\left|\widehat{X} - X\right|}{|X|} \tag{1.16}$$

$$= \frac{\left|\left(\widehat{X}_r + j\widehat{X}_i\right) - \left(X_r + jX_i\right)\right|}{\left|X_r + jX_i\right|} \tag{1.17}$$

$$= \sqrt{\frac{\left(\widehat{X}_r - X_r\right)^2 + \left(\widehat{X}_i - X_i\right)^2}{X_r^2 + X_i^2}} \tag{1.18}$$

where $\widehat{X}$ identifies the synchrophasor estimated by the PMU, X the true one and the subscripts r and i identify the real and imaginary parts of the synchrophasor respectively.

The TVE can be used to set the PMU accuracy requirements by defining the maximum allowable limit like any other error quantity. It can be visualized as a circle centered around the true synchrophasor X characterized by a radius corresponding to the maximum allowable TVE error (that also correspond to the maximum allowable magnitude error). If the estimated synchrophasor falls within the circle the PMU is compliant else it is not (see Figure1.6).
Treating a single number to characterize the PMU accuracy in estimating the synchrophasor has its advantages and disadvantages. Among the latter, the impossibility to decouple the contribution of amplitude and phase estimation error to understand eventual PMU asymmetries in the synchrophasor estimation. For these reasons in what follows the TVE will be considered together with the amplitude and phase errors as additional metrics.

Frequency Error

The Frequency Error (FE) is defined in the IEEE Std C37.118 [1] as follows:

$$FE \triangleq \left| f - \widehat{f} \right| \tag{1.19}$$

being f the true frequency value and $\widehat{f}$ the one estimated by the PMU.

ROCOF Error

The Rate of Change Frequency Error (RFE) is defined in the IEEE Std. C37.118 [1] as follows:

$$RFE \triangleq \left| ROCOF - \widehat{ROCOF} \right| \tag{1.20}$$

being $ROCOF$ the true ROCOF value and $\widehat{ROCOF}$ the one estimated by the PMU.

Magnitude Error

The Magnitude Error (ME) is defined as follows:

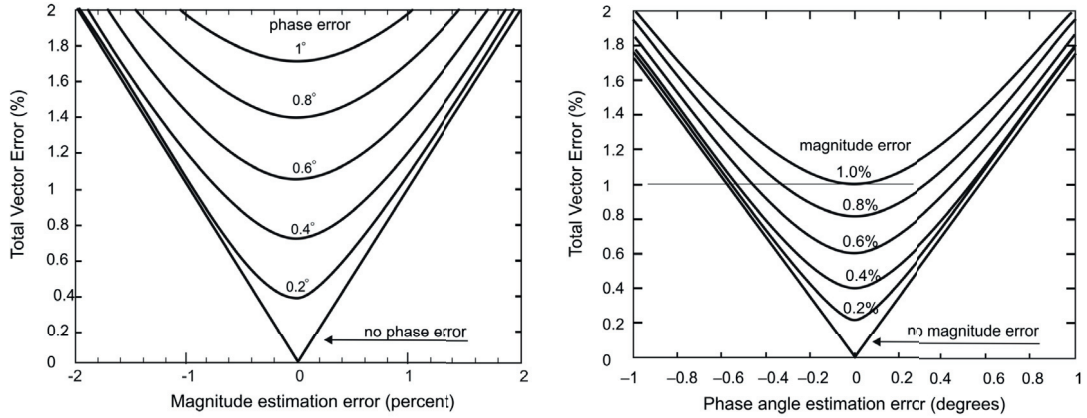
$$\varepsilon_A \triangleq A - \widehat{A} \tag{1.21}$$

being A the true magnitude of the signal and $\widehat{A}$ the one estimated by the PMU.
The TVE can be expressed in function of the magnitude estimation error only and its behavior is depicted in Figure 1.7a for various phase errors.

Phase Error

The Phase Error (PE) is defined as follows:

$$\varepsilon_\psi \triangleq \psi - \widehat{\psi} \tag{1.22}$$



(a) TVE as a function of the magnitude error only for various phase errors.

(b) TVE as a function of the phase error only for various magnitude errors.

Figure 1.7 – TVE as a function of the phase error (a) and magnitude estimation error (b) only (adapted from [1]).

being ψ the true instantaneous phase of the signal and $\widehat{\psi}$ the one estimated by the PMU. The TVE can be expressed in function of the phase estimation error only and its behavior is depicted in Figure 1.7b for various magnitude errors.

Response Time

The response time (RT) is defined as the transition time between two consecutive steady state measurements, before and after a step change is applied at one or more waveforms acquired by the PMU.
It is evaluated by applying a step change in the amplitude or phase of the input waveforms and measuring the time interval where the PMU errors exceed some predefined accuracy limits (see Figure 1.8). If t_{start} is the time of the first PMU estimation that exceed the limit and t_{end} is the time of the first PMU estimation that reenters and stays within that limit, then the response time can be computed as:

$$RT \triangleq t_{end} - t_{start} \tag{1.23}$$

The evaluation of the response time is useful to understand the effect of the adopted window length during power system transients.

Delay time

The delay time is defined as the time interval between the instant that a step change is applied to the input of a PMU and measurement time that the stepped parameter achieves a value that is halfway between the initial and final steady-state values [1].

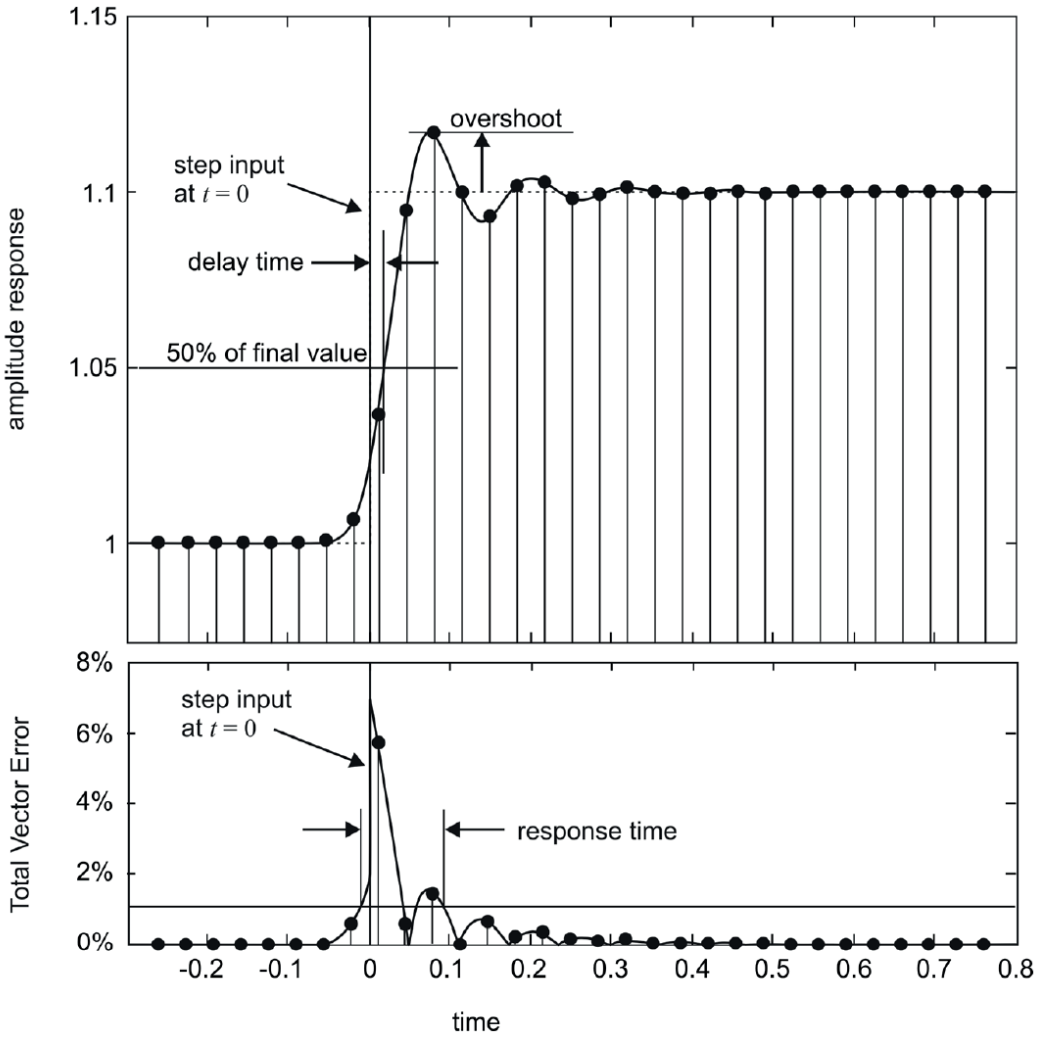


Figure 1.8 – Representation of the PMU response time, delay time and maximum overshoot during an amplitude step change with a TVE limit of 1% (adapted from [1]).

It is evaluated by applying a step change in the amplitude or phase of the input waveforms and measuring the time interval between the effective time the step change takes place and the moment the PMU estimation of the stepped parameter reached a value that is halfway between the initial and final steady-state values (see Figure 1.8).
The evaluation of the delay time is useful to verify that the time-stamp has been properly compensated for any delay introduced by the PMU filtering system.

Maximum Overshoot

The maximum overshoot is defined as the measure of the maximum peak value of the estimated synchrophasor by the PMU during a step change of the instantaneous amplitude or phase (see Figure 1.8).

Table 1.2 – The IEEE Std. C37.118 compliance requirements for steady-state conditions (in the table F_s is the PMU reporting rate). The symbol "-" means that either the specific performance class does not include that specific test or that the specific requirements has been suspended by the IEEE Std. C37.118 amendment [8].

Influence quantity		**TVE [%]**		**FE [Hz]**		**RFE [Hz/s]**	
		P-class	M-class	P-class	M-class	P-class	M-class
Signal Frequency	-	1	1	0.005	0.005	0.4	0.1
Signal Magnitude	-	1	1	0.005	0.005	0.4	0.1
Harmonic Distortion	$F_r > 20$	1	1	0.005	0.025	0.4	-
	$F_r \leq 20$	1	1	0.005	0.005	0.4	-
OOB Interference	-	-	1.3	-	0.01	-	-

Reporting Latency

The reporting latency is the time delay between the time a specific event has occurred in the power system and the time it is measured and reported by the PMU. The main contribution to this quantity are: (i) the adopted window length, (ii) the processing time needed by the synchrophasor estimation algorithm and (iii) the processing time needed by the encapsulation and streaming process (see Figure 1.2).
It is typically measured by connecting the PMU point-to-point with a PMU calibrator that has the possibility to time-tag the moment a PMU data frame is received at its network adapter. By assuming the network delays negligible, the reporting latency can be computed as follows:

$$RL \triangleq t_r - t_s \tag{1.24}$$

being t_s the PMU time stamp of a specific data frame and t_r the time that data frame has been received in the calibrator.
The maximum allowable reporting latencies are independent of the testing conditions and equal to $2/F_r$ and $7/F_r$ for P-class and M-class respectively, being F_r the PMU reporting rate.

1.3.4 The Steady-state Compliance Tests

Steady state conditions are defined as conditions where the instantaneous parameters of the reference signals (including also the parameters of the interfering signals other then the main tone) are constant along the whole duration of each sub-test. According to [1], the PMU steady state compliance can be accomplished by satisfying the accuracy requirements for TVE, FE, and RFE of the specific performance class, while varying the influence quantities that are listed below. Table 1.2 summarize the IEEE Std. C37.118 [1] steady-state compliance limits (including the latest amendment reported in [8]) for TVE, FE and RFE for both performance classes P and M.

Signal Frequency

During this test, the reference signals are composed by a single sinusoidal component characterized by a frequency f that is varied by 0.1 Hz between each sub-test, whereas the other tone parameters (A and φ) are kept constant. The frequency bandwidth to be tested depends on the targeted performance class and reporting rate but cannot be higher than 10 Hz, centered around the nominal frequency f_0 (e.g., in the case of a nominal frequency of 50 Hz, the widest frequency range to be tested is between 45 and 55 Hz).

Signal Magnitude (voltage and current)

During this test, the reference signal is composed by a single sinusoidal component characterized by an amplitude A that is varied by 10% between each sub-test, whereas the other tone parameters (f and φ) are kept constant. The amplitude range to be tested depends on the targeted performance class and whether the measured quantity is a voltage or a current. In general it cannot be lower than 10% of the nominal amplitude A_0 and higher than 120% of A_0 for voltage signals or 200% of A_0 for current signals.

Harmonic Distortion

This test allows to assess the influence of harmonics on the quality of the estimated synchrophasor, frequency and ROCOF. It assumes that a steady-state single tone signal at the nominal frequency f_0 and characterized by a nominal amplitude A_0 is corrupted by a single superposed harmonic characterized by an amplitude that is either 1% or 10% of the nominal amplitude A_0 in case of P-class or M-class compliance respectively. The harmonic order is varied between each test, starting from the 2^{nd} up to the 50^{th} harmonic.

Out-of-band (OOB) Interference

This test allows to assess the influence of inter- and sub-harmonics on the quality of the estimated synchrophasor, frequency and ROCOF and it is only defined for M-class compliance. Out-of-band compliance must be tested with a main tone signal characterized by a frequency within $f_0 - 0.1F_r/2$ and $f_0 + 0.1F_r/2$, being F_r the reporting rate and $F_r/2$ the associated Nyquist limit (e.g. between 47.5 and 52.5 Hz if f_0 is 50 Hz) and a nominal amplitude A_0. Single inter- or sub-harmonic signals must be superposed to such a main tone and be characterized by an amplitude equal to 10% of A_0 and a frequency that is either within 10 Hz and $f_0 - F_r/2$ or within $f_0 + F_r/2$ and $2f_0$.

1.3.5 The Dynamic Compliance Tests

Dynamic conditions are defined in [1] as conditions where the instantaneous parameters of the main tone of the reference signal (namely its frequency f, amplitude A and initial phase

Table 1.3 – The IEEE Std. C37.118 limits for TVE, FE and RFE during dynamic conditions (in the table F_m is the maximum modulating frequency for a specific PMU reporting rate F_r).

Test	**TVE [%]**		**FE [Hz]**		**RFE [Hz/s]**	
	P-class	M-class	P-class	M-class	P-class	M-class
Measurement Bandwidth	3	3	$0.03F_m$	$0.06F_m$	$0.18\pi F_m^2$	$0.18\pi F_m^2$
Frequency Ramp	1	1	0.01	0.01	0.4	0.2
Amplitude/Phase Steps	1	1	0.005	0.005	0.4	0.1

φ) are not constant along the duration of each sub-test. Therefore, with the term dynamic conditions, the IEEE Std. [1] does not include the evaluation of the PMU performances during dynamic behavior of any interfering signals. According to [1], the PMU dynamic compliance can be accomplished by satisfying the accuracy requirements for TVE, FE, and RFE together those for the response time for the specific performance class, during the following tests.

Measurement Bandwidth

This test aims at testing the quality of the PMU estimations during increasing variation of the instantaneous amplitude $A(t)$ and phase $\psi(t)$ of the main tone of the reference signal. In particular, during this test the reference signals are characterized by independent sinusoidal amplitude or phase modulations according to the following formula:

$$x(t) = A_0\left[1 + k_a \cos\left(2\pi f_m t\right)\right] \cdot \cos\left[2\pi f_0 t + k_p \cos\left(2\pi f_m t - \pi\right)\right] \tag{1.25}$$

being f_m the modulating frequency, k_a and k_p the amplitude and modulation factors respectively. According to [1] f_m must be varied by steps of 0.2 Hz or smaller between each sub-test, within a range that goes from 0.1 to $F_m \triangleq \min(F_r/10, 2)$ or from 0.1 to $F_m \triangleq \min(F_r/10, 5)$ in the case of P-class or M-class compliance respectively. On the other hand, the modulation factors k_a and k_p are set constant to 0.1 and the two modulations applied separately.

System Frequency Ramp

This test is defined to verify the correct positioning of the time-stamp within the time-window and to test the linearity of the PMU "filter". During this test, the main tone parameters are kept constant except the instantaneous frequency that is varied linearly with a constant rate of 1 Hz/s. Both positive and negative ramps must be tested within a frequency range that is between $f_0 - 2$ Hz and $f_0 + 2$ Hz for P-class compliance and between $f_0 - \min(F_r/5, 5)$ Hz and $f_0 + \min(F_r/5, 5)$ Hz in the case of M-class compliance.

Table 1.4 – The IEEE Std. C37.118 limits for response time during amplitude and phase steps.

Test	Phasor RT [s]		Frequency RT [s]		ROCOF RT [s]	
	P-class	M-class	P-class	M-class	P-class	M-class
Amplitude/ Phase Steps	$2/f_0$	$7/F_r$	$4.5/f_0$	$\max\left(14/F_r, 14/f_0\right)$	$6/f_0$	$\max\left(14/F_r, 14/f_0\right)$

Table 1.5 – The IEEE Std. C37.118 limits for delay time and maximum overshoot during amplitude and phase steps.

Test	Delay Time [s]		Max. Overshoot	
	P-class	M-class	P-class	M-class
Amplitude/ Phase Steps	$1/(4F_r)$	$1/(4F_r)$	$0.005A_0$	$0.01A_0$

Step Changes in Amplitude and Phase

This test is designed to simulate sudden power system events like voltage and current variations during faults, short-circuits or the synchronization of islanded/separated networks. it is aimed at testing the PMU response time, that is mainly influenced by the adopted time-window length. According to [1] the step change is applied simultaneously to all 3-phases and to both voltage and current inputs. The IEEE Std. requires to test 10% positive and negative amplitude steps and 10° positive and negative phase steps.
Tables 1.4 and 1.5 summarize the IEEE Std. C37.118 [1] dynamic compliance limits (including the latest amendment reported in [8]) for TVE, FE and RFE (see Table 1.3) together with those for the response time (see Table 1.4), delay time and maximum overshoot (see Table 1.5) for both performance classes P and M.

1.4 Scientific Literature Review

The majority of the literature regarding Phasor Measurement Unit focuses on the formulation and analysis of novel and advanced synchrophasor estimation (SE) algorithms. This is partially justified by the fact that the quality of the PMU estimations derives from a well formulated SE algorithm that takes into account as much as possible the different sources of error. Nevertheless, building up a PMU is not an easy task since it involves competencies coming from different fields, like signal processing, digital architecture design, time-synchronization etc. In what follows the most interesting scientific contribution related to PMU architectures and synchrophasor estimation algorithms will be reviewed.

1.4.1 Synchrophasor Estimation Algorithm

As discussed in [30], several algorithms for calculation of phasors and/or local system frequency and rate of change of frequency (ROCOF) have been presented in literature. In general,

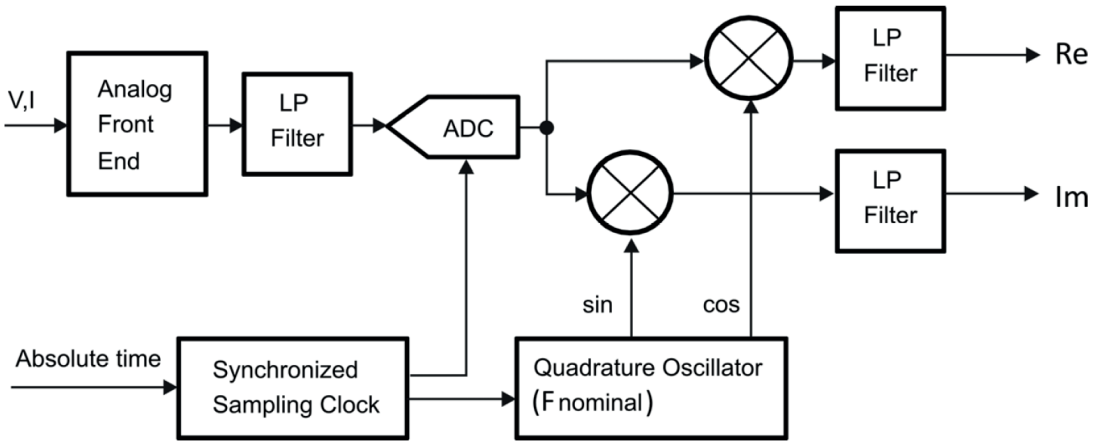


Figure 1.9 – The "reference" signal processing model based on the demodulation technique, proposed in [1].

based on the adopted signal model, they can be grouped into two categories [31]: (i) algorithms based on a *static* signal model that assume that the waveform parameters are constant within the adopted window length and (ii) algorithms based on a *dynamic* signal model that assume a more complicated but generic signal model that includes also the possibility that the waveform parameters are time-varying within the observation time window.
The majority of synchrophasor estimation methods belonging to the first category, is based on the direct implementation of the Discrete Fourier transform (DFT) [3]. Non-DFT-based synchrophasor estimation methods based on a static signal model have also been proposed along the years. These include, among others, *zero-crossing methods* [32, 33], *demodulation filters* [32, 34], *adaptive filters* [35, 36], *compressive sensing* algorithms [37, 38], *wavelet* based algorithms (e.g., [39]), *resampling* methods [40] *Prony*'s estimation methods [41] and *Matrix Pencil* methods [42].
On the other hand, most of the dynamic synchrophasor estimation algorithms (i.e., those belonging to the second category) falls within the group of the so-called Taylor-Fourier transform methods that were initiated with [43].
In what follows three of the most common synchrophasor estimation techniques, namely those based on the demodulation, Discrete Fourier Transform and Taylor Fourier Transform techniques, will be reviewed and the most relevant scientific contribution highlighted.

Demodulation

One of the first processes that has been proposed in the scientific literature to extract a synchrophasor from a given portion of voltage or current waveforms measured by a PMU is the "demodulation" method. This method is also proposed in the IEEE Std. C37.118 [1] as the reference signal processing model.
The demodulation process is based on a static signal model composed by a single frequency

component in the proximity of the nominal frequency of the power system f_0. As shown in Figure 1.9, the signal is first multiplied by the quadrature oscillator (since and cosine), then filtered by a low pass filter.
The main problem related to this technique refers to the design of suitable low pass filters with characteristics that do not affect the quality of the estimated synchrophasor. In this respect, the IEEE Std. [1] suggests specific filtering processes, and associated windows, to be adopted with respect to both P-class and M-class compliant PMUs. A detailed description of the demodulation method and definition of associated filters for synchrophasor measurements can also be found, in [35], [36] and [44].

Discrete Fourier Transform

One of the most common techniques to infer the main tone from a discrete sequence of samples of a generic input signal refers to the well known category of time to frequency domain transformations techniques. Particularly, when dealing with finite length sequence of uniformly-spaced samples of a signal, the favorite technique is definitely the Discrete Fourier Transform (DFT).
Based on the window length, several DFT-based synchrophasor estimation algorithms have been proposed in the literature and they can be grouped into multi-cycle, one-cycle, or fractional-cycle DFT estimators performing recursive and non-recursive updates (e.g., [45, 46, 47]). In order to improve their accuracy, DFT-based algorithms have been sometimes proposed in combination with weighted least-squares (e.g., [48]) or Kalman filter-based methods (e.g., [49]). Within this category, in order to reduce the effects of leakage and of the so-called picket-fence effect, the use of time-windows in combination with the well-known Interpolated-Discrete Fourier Transform (IpDFT) technique has been first proposed in [50, 51] and further developed in [52, 53, 54, 55]. More in particular, contributions [54] and [55] have proven that the effects of long and short-range leakage can be considerably minimized by adopting suitable windows functions and IpDFT schemes respectively (see also [56, 57]). The advantages of this kind of approaches refer to the relatively simple implementation and low computational complexity capable of achieving reasonable accuracy and response times after a careful selection of the algorithm parameters.

Taylor-Fourier Transform

The dynamic phasor concept proposed in [43] is a recent formulation of the SE problem that derives from the need of representing time-varying phasors. Nevertheless most of the SE techniques assume that the waveform parameters are constant, at least within the duration of a single window length (this is the case for instance of the DFT theory).
The Taylor-Fourier transform (TFT) has been introduced to overcome this limit by considering that the Fourier coefficients of the signal model are not constant and approximating their time-variation with a Taylor series truncated at a specific order. The model order is chosen as a trade-off between accuracy and computational burden [31]. In practice the TFT comes in a

form of an improved filter for a dynamic harmonic estimation of the components of a given signal. It has wider flat gains around each harmonic component and better rejection to the interference of inter-harmonics.
Some of the TFT algorithms are simply implemented as additional post-processing stage of a standard DFT-based algorithms that aims at correcting the DFT inaccuracies due to transient behaviors of the power system [58, 59, 60]. Others try to approximate the Taylor series coefficient in given observation window with a Weighted Least Squares (WLS) method [43, 61] and eventually combining this with other techniques like signal subspace [43] or adaptive filters methods [41].
In general the advantages of this group of methods with respect to the others are pretty clear and refer to the possibility of tracking (and potentially estimating) the power system dynamics. On the other hand a non-negligible drawback is related to the computational complexity of this kind of methods that generally tends to be higher. Additionally it is barely impossible to track any kind of dynamics. In particular sudden ones, like those happening during faults, still deteriorate the quality of the estimated synchrophasor for the duration of the window length, that is typically quite high in the case of TFT algorithms.

1.4.2 PMU prototyping and metrological characterization

Few of the above-listed works have focused on the deployment of the proposed SE algorithm into a real PMU prototype. Among them in [53] Paolone et al. discussed the deployment of an IpDFT algorithm into an RTU based on a micro-controller platform that processes a set of data collected on an FPGA. Although the proposed PMU prototype could not estimate more than 10 synchrophasors per second per each channel (up to a maximum of 6 channels), [11] has demonstrated the applicability of such a technique to the real-time monitoring of an islanding maneuver of an Active Distribution Network. Similarly, Castello et al. propose in [62] a novel Intelligent Electronic Device (IED) architecture with PMU functionalities that can be used to monitor electrical distribution networks. Such a contribution was on of the first to discuss the possibility of synchronizing the PMU estimations using the IEEE Std 1588-2008 for precise time synchronization over telecom networks. This work has been extended in [63] including the integration and the performance analysis of a Wireless Redundant Process bus for the data transmission. Another relevant contribution is also the one presented by Laverty et al. in [64] where the OpenPMU project is presented, one of the few open platforms capable to host a PMU device.
Some contributions have also analyzed the influence of the time-synchronization reliability on the PMU estimations. These include [65, 66] where the effect of GPS spoofing and time synchronization attacks on PMUs are evaluated.
Finally some works have discussed the PMU metrological characterization. Among them, [67] and [68] discuss the static and dynamic PMU calibration performed at the National Institute of Standards and Technology (NIST) whereas [69] presents the architecture and characterization of a calibrator for PMUs operating in power distribution systems.

2 PMU Accuracy Requirements for ADNs Monitoring

This Chapter is meant to quantify the accuracy requirements of PMUs expected to operate in ADNs and analyze the inadequacy of the IEEE Std. C37.118 [1] when applied to the design and testing of this kind of devices. Due to the high amount of power-system applications that can exploit the availability of PMUs at such a voltage level, the analysis will focus on a specific PMU application, namely ADNs monitoring. In particular, the steady-state requirements are derived from the results of computer simulations designed to evaluate typical operating conditions of ADNs. This analysis will be also enriched by some considerations on potential waveform distortions according to the most up-to-date literature on the subject.

2.1 Derivation of the PMU Requirements

The accuracy requirements for PMUs operating in ADNs have not been defined yet in any international standard. Indeed the PMU technology has been historically developed for transmission network monitoring and, just lately, has emerged as a potential candidate for the real-time monitoring and control of ADNs and microgrids. In this respect, the application of such a technology at the power distribution level is still in a preliminary and experimental phase where few available pilots are trying to demonstrate the applicability of the current PMU technology to monitor, and eventually control, ADNs. For this reason, the main efforts towards the definition of requirements for PMUs operating in ADNs are still addressed by the research stage rather than standardization bodies.
As already discussed in Section 1.3, the PMU performances and related requirements are expressed in terms of two figures of merit: (i) accuracy and (i) reporting latency. The latter is defined as the amount of time the PMU takes to report a specific event and is univocally measured as the time difference between the instant an event has taken place in the power system and the moment the same event is reported by the PMU (see Section 1.3.3). On the other hand, the former is defined as the discrepancy between the PMU measurements and the corresponding “true” value of the measured quantity and can be evaluated based on several

metrics. In this respect the IEEE Std. C37.118 [1] has defined TVE, FE and RFE to evaluate the PMU accuracy in both steady-state and dynamic conditions and the delay time and response time to evaluate the PMU response to step changes (see Chapter 1).
The PMU accuracy and latency requirements should be derived, like any other measurement device, from the desired performances of the application that will make use of the measurement data. Nevertheless, such a standard approach has an intrinsic limitation when applied to synchrophasors, as the amount of power-system applications that can exploit the availability of PMU data is considerable and continuously increasing. In this respect, recently the North American Synchrophasor Initiative (NASPI) has released the first version of a technical study called *The Synchrophasor Starter Kit* [70] that, among others, has identified a set of essential application for a transmission system operator (TSO). These have been grouped in two main categories, namely power-system *monitoring* and *protections*. The former category includes:

- Model validation;
- Event analysis;
- Frequency monitoring;
- Phase angle monitoring;
- Voltage monitoring;
- Asset management, equipment mis-operation and system health monitoring;
- Equipment commissioning
- Energy Management System (EMS) backup;
- Linear state estimation
- Wide area situational awareness;
- Data conditioning;

and the latter:

- Breaker reclosing with phase angles;
- Automated special protection schemes;
- Islanding;
- Fault identification and location.

For ADNs a similar list can be derived. This will include, in addition to these two categories, a third one, namely power-system *control*, that includes a group of applications that has lately emerged together with the increasing penetration of DERs (i.e., RERs and storage mainly) in the power distribution infrastructure [71, 72]. It is therefore evident that the major obstacle in defining the PMU requirements is related to the large variety and amount of applications to be considered with respect to ADNs.
Additionally, it is important pointing out that the required PMU accuracy is not only influenced by the related application performances, but also by the peculiar characteristics and operating conditions of the electrical grid where the PMU will be installed. In particular, the accuracy requirements for PMUs operating at power distribution level are usually more demanding than those for PMUs installed in power transmission systems.
The IEEE Std. C37.118 has simplified such an analysis. It has focused only on two performance classes, namely P-class for protection and M-class form measurement applications and derived the related accuracy requirements for the case of transmission networks only. In particular, for P-class PMUs the IEEE Std. [1] has identified more stringent response time and measurement reporting latency requirements, according to the typical latency requirements of the existing relay-based approaches. On the other hand, for M-class PMUs these limits are more relaxed and the focus is more on the PMU measurement accuracy.
Although the IEEE Std. C37.118 has the merit of being the first attempt towards the definition of such requirements, the distinction presented in [1] seems too simplistic for the following reasons:

- it is quite ambiguous how the accuracy and latency requirements have been derived and particularly how they have been associated to the two considered power-system applications;
- it does not make difference between requirements for PMUs operating in transmission and distribution networks;
- it assumes that applications requiring fast response do not require accuracy and vice versa, whereas there are applications where both parameters are crucial (see for instance emerging applications of PMUs to Wide Area Protection Systems [73, 74, 75])
- it has considered only 2 categories of power-system applications, namely power system monitoring and protections, and has neglected power-system control applications.

Additionally, as discussed in Section 2.3, the IEEE Std. C37.118 test suite does not take into account every possible distortion that can be included in the processed waveforms.
Within this context, the following of the Chapter will focus on the definition of the accuracy requirements for PMUs expected to operate in ADNs and will derive them for the group of applications belonging to the power-system monitoring category. The benefits related to this group of applications refer to the capability of correctly measure in real-time the voltage and current phasor (i.e., active and reactive power) variations in an electrical network.

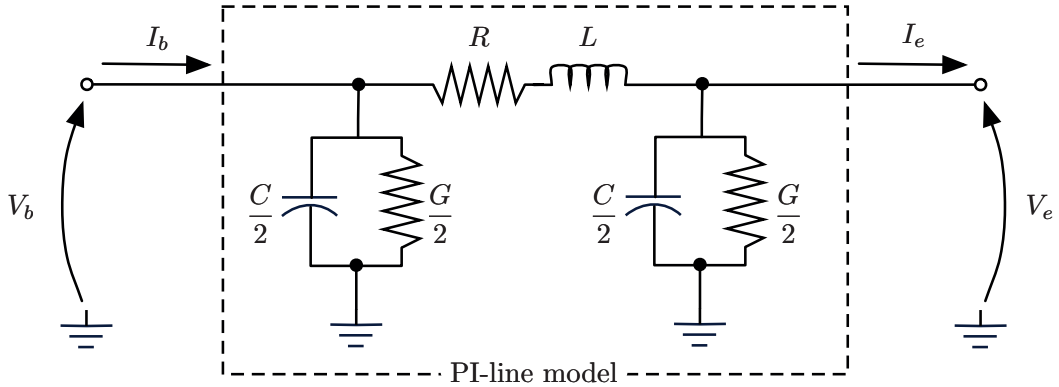


Figure 2.1 – Adopted PI-line model of a transmission line that also highlights the current sign convention. The model is uniquely identified by fixing the electrical parameters R, L, C, G of the line.

The Chapter will only focus on the PMU accuracy requirements as the measurement reporting latency limits are, in real-applications, not only influenced by the PMU performances but also by the adopted telecommunication infrastructure that transports the synchrophasor data. Additionally they are typically straightforward to be derived based on the latency requirements of current solutions (see [76] for an extensive treatment of the required latency for a group of standard power system applications).

2.2 Steady-state Accuracy Requirements

Compared to transmission networks, ADNs are characterized by shorter line lengths (5-10 kilometers maximum), lower feeder impedances (in the order of few hundreds mΩ/km) and reduced power flows (in the order of few MW or even less depending in the specific time of the day). These characteristics result in amplitude and angle differences between bus voltage and line current synchrophasors that never exceed few degrees (typically even lower than one degree).
The following of this Section is meant to evaluate these phasor differences and derive the required accuracy limits for PMUs operating in ADNs.

2.2.1 Simulation Setup

In order to evaluate such behavior, a simple but at the same time representative single-phase model of a transmission line has been considered[1]. As known, transmission lines of short- and medium-length are well represented by the two-port π-model (or PI-model) represented in Figure 2.1 [77]. This is uniquely identified by fixing the line length λ, its series (or longitudinal)

[1] The same results can be obtained by considering a balanced three-phase model of a transmission line.

impedance z:

$$z = r + j\omega l = r + jx \tag{2.1}$$

and its shunt (or transverse) admittance y:

$$y = g + j\omega c = g + jb, \tag{2.2}$$

being:

- $r = R/\lambda$ [Ω/m] the line resistance per unit length;
- $l = L/\lambda$ [H/m] the line inductance per unit length;
- $g = G/\lambda$ [S/m] the line conductance per unit length;
- $c = C/\lambda$ [F/m] the line capacitance per unit length;
- $\omega = 2\pi f_0$, being f_0 the nominal frequency of the power system (50 or 60 Hz).

With these assumptions and the current sign convention depicted in Figure 2.1, the voltage and current phasors at the beginning of the line (V_b, I_b) can be expressed as a function of the voltage and current phasors at the end of the line (V_e, I_e) using the two-ports equivalent model of the line:

$$\begin{bmatrix} V_b \\ I_b \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_e \\ I_e \end{bmatrix} \tag{2.3}$$

where the parameters A, B, C, D of the auxiliary matrix of the two-ports equivalent of the circuit shown in Figure 2.1 can be calculated as follows:

$$A = \cosh(\gamma\lambda) \tag{2.4}$$
$$B = Z_0 \sinh(\gamma\lambda) \tag{2.5}$$
$$C = \frac{1}{Z_0} \sinh(\gamma\lambda) \tag{2.6}$$
$$D = A \tag{2.7}$$

being γ the propagation constant:

$$\gamma = \sqrt{z \cdot y} \tag{2.8}$$

and Z_0 the characteristic impedance of the line:

$$Z_0 = \sqrt{\frac{z}{y}}. \tag{2.9}$$

During each simulation the voltage and current phasors at the end of the line are fixed to:

$$V_e = \frac{(V_n + j0)}{\sqrt{3}} \tag{2.10}$$

$$I_e = \left(\frac{P_e + jQ_e}{V_e}\right)^* \tag{2.11}$$

being V_n the nominal phase-to-phase voltage of the power system. The complex power at the end of the line $P_e + jQ_e$ can be simply derived from the apparent power S_e once the power factor is fixed:

$$P_e = S_e \cdot \cos\varphi \tag{2.12}$$

$$Q_e = S_e \cdot \sin\varphi. \tag{2.13}$$

The voltage and current phasors at the beginning of the line are derived according to equation (2.3) and the amplitude and phase angle differences between the voltage and current phasors at the two extremities of the line computed as follows:

$$\varepsilon_{V,m} = |V_b| - |V_e| \tag{2.14}$$

$$\varepsilon_{V,p} = \angle V_b - \angle V_e \tag{2.15}$$

$$\varepsilon_{I,m} = |I_b| - |I_e| \tag{2.16}$$

$$\varepsilon_{I,p} = \angle I_b - \angle I_e \tag{2.17}$$

where the subscripts m and p identify the magnitude and phase angle differences.

2.2.2 Simulation Results

In order to evaluate the amplitude and phase angle differences between bus voltage and line current phasors at the beginning and at the end of the line, several simulation where performed by fixing the nominal frequency $f_0 = 50$ Hz and varying the following parameters:

- the nominal voltage $|V_e|$ at the end of the line;
- the line load, namely the apparent power $S_e = \left|P_e + jQ_e\right|$ at the end of the line;
- the power factor $\cos\varphi$ at the end of the line, namely the ratio between active and reactive power;
- the line length λ;
- the line type, namely its parameters r, c, l, g.

The previously mentioned parameters have been varied in the ranges shown in Table 2.1 and every possible combination of them has been evaluated. Therefore, eight groups of plots have been obtained, namely:

Table 2.1 – Considered operating conditions of the analyzed transmission line.

Nominal voltage	**Apparent power**	**Power factor**	**Line length**	**Line type**
4.16 kV, 20 kV	0.001 ÷ 1500 kVA	0.9, 0.5	10 ÷ 5000	cable, overhead
Line type	r [Ω/m]	g [S/m]	l [H/m]	c [F/m]
cable	$0.0995 \cdot 10^{-3}$	$0.285 \cdot 10^{-9}$	$0.309 \cdot 10^{-6}$	$0.302 \cdot 10^{-9}$
overhead	$0.268 \cdot 10^{-3}$	0	$1.1 \cdot 10^{-6}$	$0.0107 \cdot 10^{-9}$

- Figure 2.2 showing the simulation results for a cable line, with nominal voltage $V_n = 20$ kV, and a power factor $\cos\varphi = 0.9$;
- Figure 2.3 showing the simulation results for a cable line, with nominal voltage $V_n = 20$ kV, and a power factor $\cos\varphi = 0.5$;
- Figure 2.4 showing the simulation results for an overhead line, with nominal voltage $V_n = 20$ kV, and a power factor $\cos\varphi = 0.9$;
- Figure 2.5 showing the simulation results for an overhead line, with nominal voltage $V_n = 20$ kV, and a power factor $\cos\varphi = 0.5$;
- Figure 2.6 showing the simulation results for a cable line, with nominal voltage $V_n = 4.16$ kV, and a power factor $\cos\varphi = 0.9$;
- Figure 2.7 showing the simulation results for a cable line, with nominal voltage $V_n = 4.16$ kV, and a power factor $\cos\varphi = 0.5$;
- Figure 2.8 showing the simulation results for an overhead line, with nominal voltage $V_n = 4.16$ kV, and a power factor $\cos\varphi = 0.9$;
- Figure 2.9 showing the simulation results for an overhead line, with nominal voltage $V_n = 4.16$ kV, and a power factor $\cos\varphi = 0.5$.

In particular, the simulation results are shown in form of 2D graphs where the nominal voltage, power factor and line parameters are fixed, whereas the line load (x-axis) and line length (y-axis) are varied in the range $0.001 \div 1500$ kVA and $10 \div 5000$ meters respectively. In this respect, within each group of graphs, Figures (a) and (b) show the magnitude differences for voltage ($\varepsilon_{V,m}$ [V]) and current ($\varepsilon_{I,m}$ [A]) phasors, whereas Figures (c) and (d) show the phase angle differences for voltage ($\varepsilon_{V,p}$ [rad]) and current ($\varepsilon_{I,p}$ [rad]) phasors.
On the other hand Figures (e) and (f) report the equivalent Total Vector Difference (TVD) for both voltage and current phasors. This quantity has been derived, similarly to the TVE defined in equation (1.16), from the voltage and current phasor differences at the beginning and the end of the line, normalized with respect to the amplitude of the voltage and current phasors at

the end of the line (as this is the quantity that is fixed in each simulation):

$$TVD_V = \frac{|V_b - V_e|}{|V_e|} = \sqrt{\frac{\left(V_{b,r} - V_{e,r}\right)^2 + \left(V_{b,i} - V_{e,i}\right)^2}{V_{e,r}^2 + V_{e,i}^2}}, \tag{2.18}$$

$$TVD_I = \frac{|I_b - I_e|}{|I_e|} = \sqrt{\frac{\left(I_{b,r} - I_{e,r}\right)^2 + \left(I_{b,i} - I_{e,i}\right)^2}{I_{e,r}^2 + I_{e,i}^2}}. \tag{2.19}$$

By analyzing the obtained graphs, the following remarks can be made:

- Independently of the considered nominal voltage, power factor and line type, graphs (a), (b), (c) and (d) of each Figure always show the same patterns. In particular, as expected the voltage magnitude and phase differences are influenced by both line length and line load and become smaller as the line gets shorter and/or the power flow smaller. However current phasor differences, i.e. graphs (b) and (d), exhibit a different behavior that can be justified by taking into account the effects of the reactive power balance between the line and the power source on the current phasors[2]. In particular the current magnitude differences are mainly influenced by the line length, and gets smaller for shorter line lengths. On the other hand the current phase angle differences are bigger for longer lines with lower loads and get smaller by increasing the line load and reducing its length. By looking at graphs (e) and (f), it is evident how the voltage TVD exhibits the same pattern as the one of the magnitude and phase angle differences, whereas the current TVD is mostly affected by the pattern characterizing the phase angle differences.
- Independently of the considered nominal voltage and line type, the power factor effects on amplitude and phase angle differences (i.e., on the related TVD) are negligible. They are slightly more evident when considering an overhead line rather then a cable line. In this case, the power factor mainly affect the phase angle difference between voltage phasors and the magnitude differences between current phasors.
- Independently of the considered nominal voltage and power factor, the line type (i.e., the parameters of the cable or overhead lines) influences the relative differences between voltage and current phasors. With overhead lines, the voltage magnitude and phase angle differences are usually bigger than the same differences obtained with cable lines. On the other hand with cable lines, the current magnitude and phase differences are usually larger than in the case of overhead lines. This also affects the related TVD values.
- Independently of the considered power factor and line type, the nominal voltage directly affects the phase angle separation between both voltage and current phasors. This is evident, for instance, by looking at Figures 2.2 and 2.6. The first Figure, obtained for a nominal voltage of 20 kV, exhibits bigger magnitude and phase angle differences between voltage phasors at the two line extremities compared to the second. On the

[2]It should not be forgotten that, independently of the load, a powered line always generates some reactive power.

other hand, the latter exhibit bigger magnitude and phase angle difference between voltage phasors at the two line extremities compared to the former Figure.

According to these graphs, the PMU requirements can be derived, once fixed the operating conditions, either from the absolute magnitude and phase angle differences between voltage and current phasors at the beginning and at the end of the line, or equivalently, from the related TVD values. It is worth pointing out that, in order to constraint the PMU accuracy to values capable to measure the obtained magnitude and phase angle differences of both current and voltage phasors at the line extremities, the obtained difference and TVD values must be reduced by, at least, a factor of 5.
The main outcome of such an analysis is that the PMU accuracy requirements for both voltage and current phasors are highly dependent on the considered operating conditions of the considered line (i.e. power grid). In other words, every considered parameter, except the power factor, has an impact on the TVE requirements and makes the voltage or current synchrophasor estimations more or less challenging. In particular:

- The parameters that are mostly influencing the PMU accuracy requirements are the line length and line load. In the case of voltage phasors, it is generally quite difficult to correctly estimate the phasors at the extremities of a line shorter than 500 meters with an apparent power flow smaller than 200 kVA. On the other hand, the correct estimation of current phasors at both ends of the line becomes more challenging with lines shorter than 200 meters and power flows higher than 500 kVA.
- The estimation of the voltage phasor differences becomes easier at lower voltages (see the case of $V_n = 4.16$ kV) as, the line load being equal, the current flow, i.e. the voltage drop, increases. On the other hand, for similar reasons, with higher nominal voltages (see for instance the case of $V_n = 20$ kV) the correct estimation of voltage phasors becomes more challenging, whereas the accuracy requirements for current phasors soften.
- The accuracy requirements on voltage phasor estimation are less demanding when considering overhead lines instead of cable lines. On the other hand, the estimations of current phasors becomes more challenging when considering overhead lines instead of cable lines.

In other words, the proposed analysis represents a tool to understand if a specific PMU technology can be applied to the real-time monitoring of current and voltage phasors of any power grid even if we limited our analysis to the values shown in Table 2.1 that are typical for ADNs. For instance, Figure 2.2e demonstrates that a PMU characterized by a maximum voltage TVE of 0.1% can correctly measure the voltage phasors of any cable line characterized by a nominal voltage of 20 kV as long as the line is longer than 2 kilometers and the apparent power flow is bigger than 500 kVA per-phase.
In general, by analyzing the obtained graphs, it is evident that an IEEE Std. C37.118 compliant

PMU (i.e., characterized by a 1% TVE) is not capable of correctly measuring neither the voltage nor the current phasors for most of the considered operating conditions. The obtained TVE graphs suggest that PMU with TVE of 0.01% and even lower are strongly suggested in ADNs.

2.3 Voltage and Current Waveform Disturbances

In an ideal power distribution system, the power would be transmitted from the primary substation to the secondary substations and connected loads through smooth AC voltage and current waveforms at the nominal frequency of the power system (i.e., 50 or 60 Hz). In such a case the analysis conducted in the previous section would be sufficient to define the accuracy requirements for PMUs operating in ADNs.
Unfortunately such hypothesis does not represent typical operating conditions of any power system, since voltage and current waveforms are typically corrupted by several kind of electromagnetic phenomena. This might be caused by periodic or a-periodic events caused by faults, non-linear loads, capacitor banks, power electronic converters, etc. In this respect the IEEE has developed the Standard 1159-2009 [15], *IEEE Recommended Practice for Monitoring Electrical Power Quality*, describing different power quality problems. In particular, [15] has identified seven kind of power quality disturbances, depending on their spectral contents, durations and voltage magnitudes:

- *Transient events*, characterized by an extremely high spectral content and very short durations (few ms maximum);
- *Power interruptions*, characterized by duration that can go up to some minutes;
- *Voltage sags or brownouts* (also called undervoltages), namely sudden reductions of the AC voltage RMS that might last from few hundreds of ms up to some minutes;
- *Voltage swells or overvoltages*, namely sudden increase of the AC voltage RMS that might last from few hundreds of ms up to some minutes;
- Steady-state *waveform distortions*, including DC offset, harmonics, inter-harmonics, notching and broadband noise;
- *Voltage fluctuation* with very slow frequencies in the order of few Hz;
- Power frequency variations in the range $f_0 \pm 0.1$ Hz.

As already discussed in Section 1.3, the IEEE Std. C37.118 compliance verification has been designed around a suite of tests that include, besides a basic test aimed at assessing the PMU accuracy with ideal single tone signals, a quite significant group of tests aimed at assessing the PMU performances in presence of waveform distortions and dynamic events. In particular, with respect to the list of power quality disturbances listed in [15] The IEEE Std. [1] has defined (see Section 1.3):

- the step tests to verify the PMU accuracy with voltage and current waveforms that emulate those taking place during *power interruption* events, *voltage sags* or *swells*;
- the frequency ramp tests to evaluate the PMU performances when processing voltage and current waveforms undergoing a linear *frequency variation*;
- the measurement bandwidth test to emulate slow *fluctuations* of the amplitude and phase of voltage and current waveforms;
- the harmonic distortion and OOB interference tests to evaluate the effects of *harmonics* and *inter-harmonics* on the PMU accuracy.

In this respect, it is evident how the IEEE Std. C37.118 [1] has on purpose excluded the PMU accuracy assessment during transient event, as the theoretical bandwidth of PMUs would not allow the measurement of this kind of dynamics. On the other hand, it is not justified the absence of dedicated tests aimed at verifying the PMU performances with:

- harmonic or inter-harmonic signals superposed to a main tone characterized by a frequency that is fluctuating around the nominal frequency of the power system f_0;
- superposed wideband noise;
- superposed decaying DC offset with different time constants.

In this regard, the metrological characterization of the proposed PMU prototype, will consider these additional disturbances and metrologically assess the PMU performances with these kind of signals. In particular, the testing conditions regarding the presence of harmonics have been derived by from the European Voltage Disturbances Standard EN 50160 (Voltage Characteristics in Public Distribution Systems).
Ideally, during these events, a PMU must satisfy the same accuracy requirements derived in Section 2.2 for steady state conditions, as the differences between voltage and current phasor at the two line extremities are maintained. Nevertheless it is expected a relative deterioration of the PMU accuracies during these tests, compared to those characterized by an ideal single tone signal.

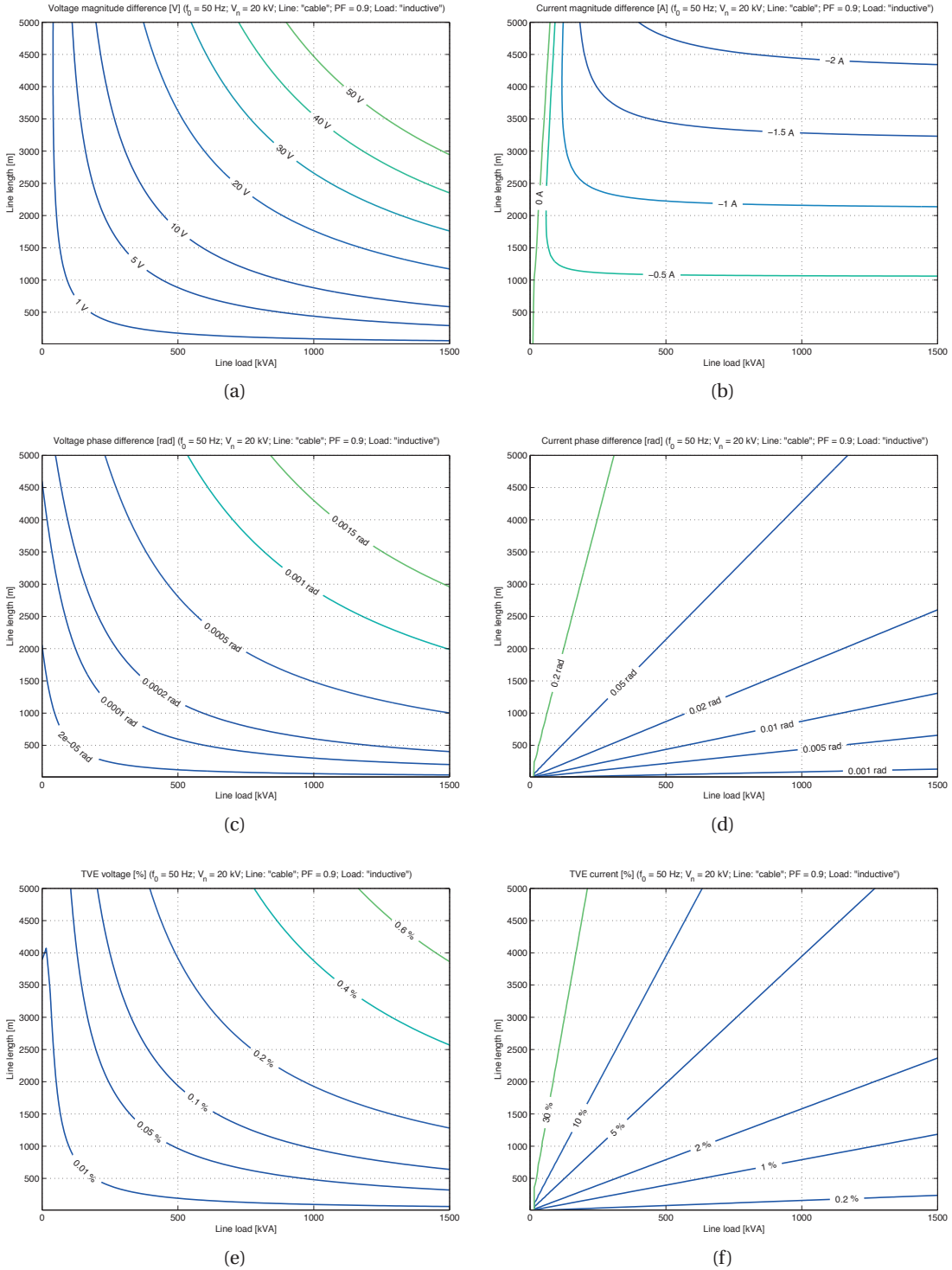


Figure 2.2 – Simulation results for a cable line, nominal voltage V_n = 20 kV, power factor $\cos\varphi$ = 0.9 showing the influence of the line load (x-axis) and line length (y-axis) on the amplitude (a,b) and phase differences (c,d) between voltage (a,c) and current (b,d) phasors measured at the beginning and at the end of a line. The related TVE requirements are derived in figures (e) and (f) for voltage and current phasors respectively.

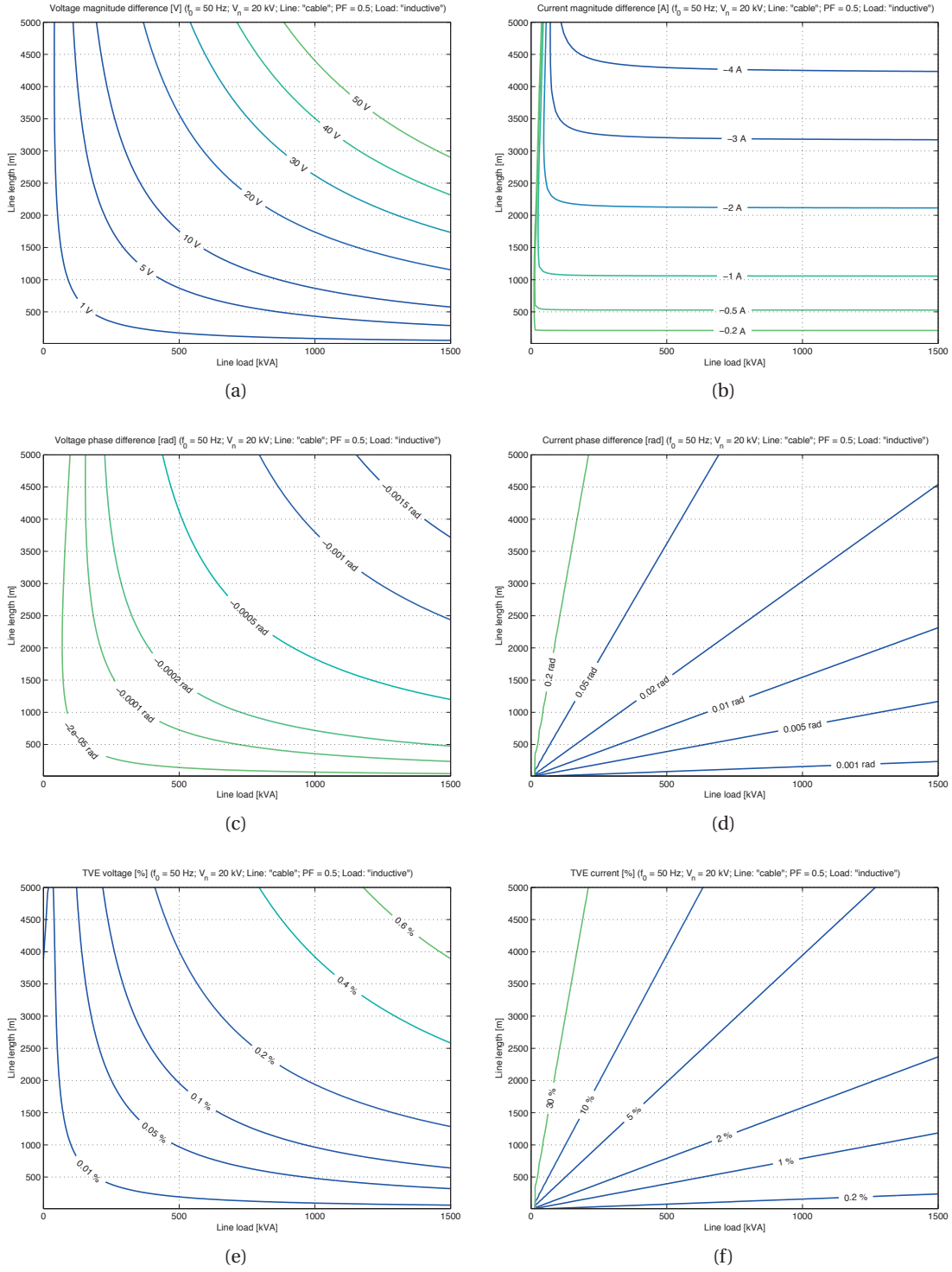


Figure 2.3 – Simulation results for a cable line, nominal voltage V_n = 20 kV, power factor $\cos\varphi$ = 0.5 showing the influence of the line load (x-axis) and line length (y-axis) on the amplitude (a,b) and phase differences (c,d) between voltage (a,c) and current (b,d) phasors measured at the beginning and at the end of a line. The related TVE requirements are derived in figures (e) and (f) for voltage and current phasors respectively.

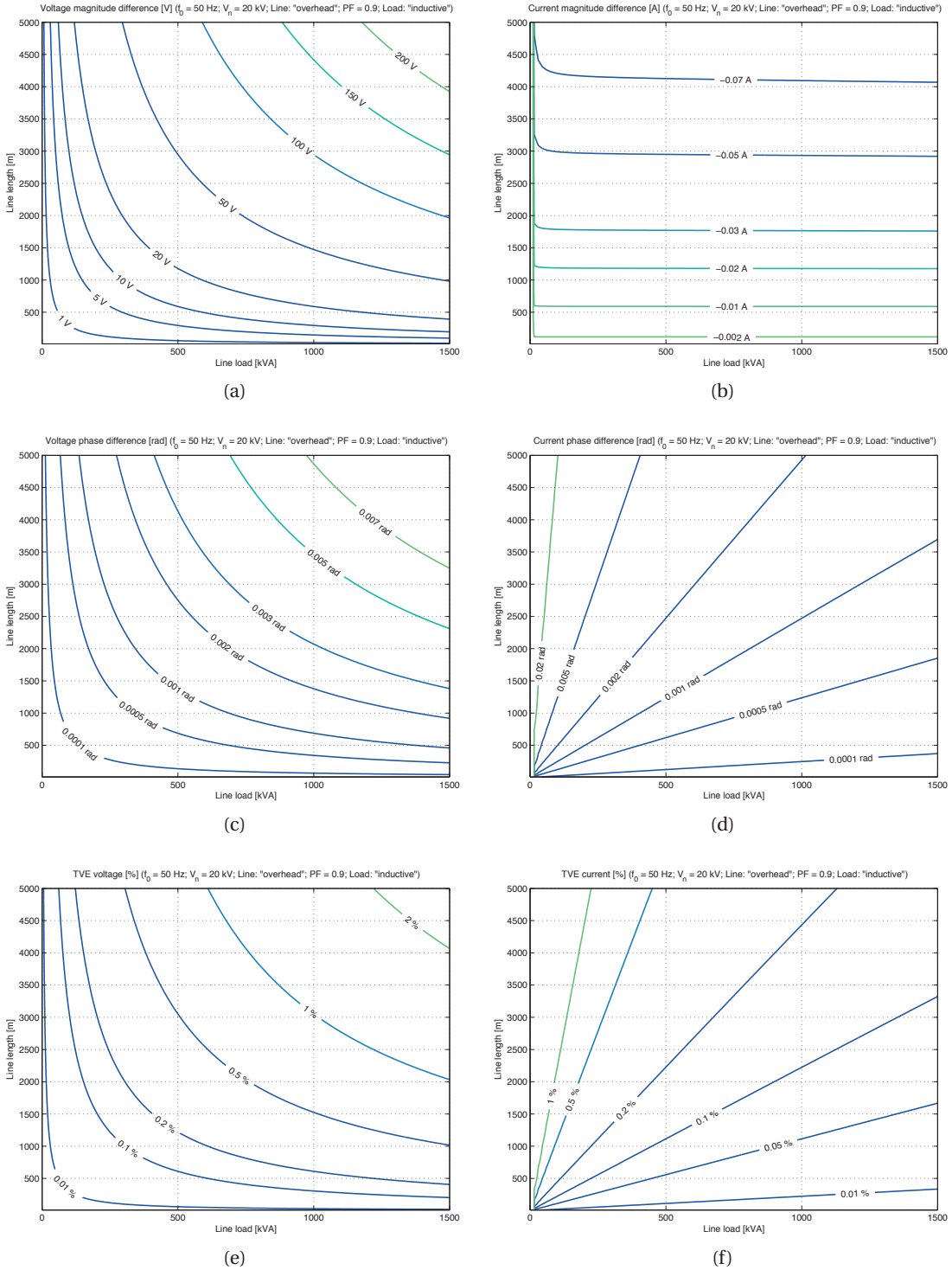


Figure 2.4 – Simulation results for an overhead line, nominal voltage $V_n = 20$ kV, power factor $\cos\varphi = 0.9$ showing the influence of the line load (x-axis) and line length (y-axis) on the amplitude (a,b) and phase differences (c,d) between voltage (a,c) and current (b,d) phasors measured at the beginning and at the end of a transmission line. The related TVE requirements are derived in figures (e) and (f) for voltage and current phasors respectively.

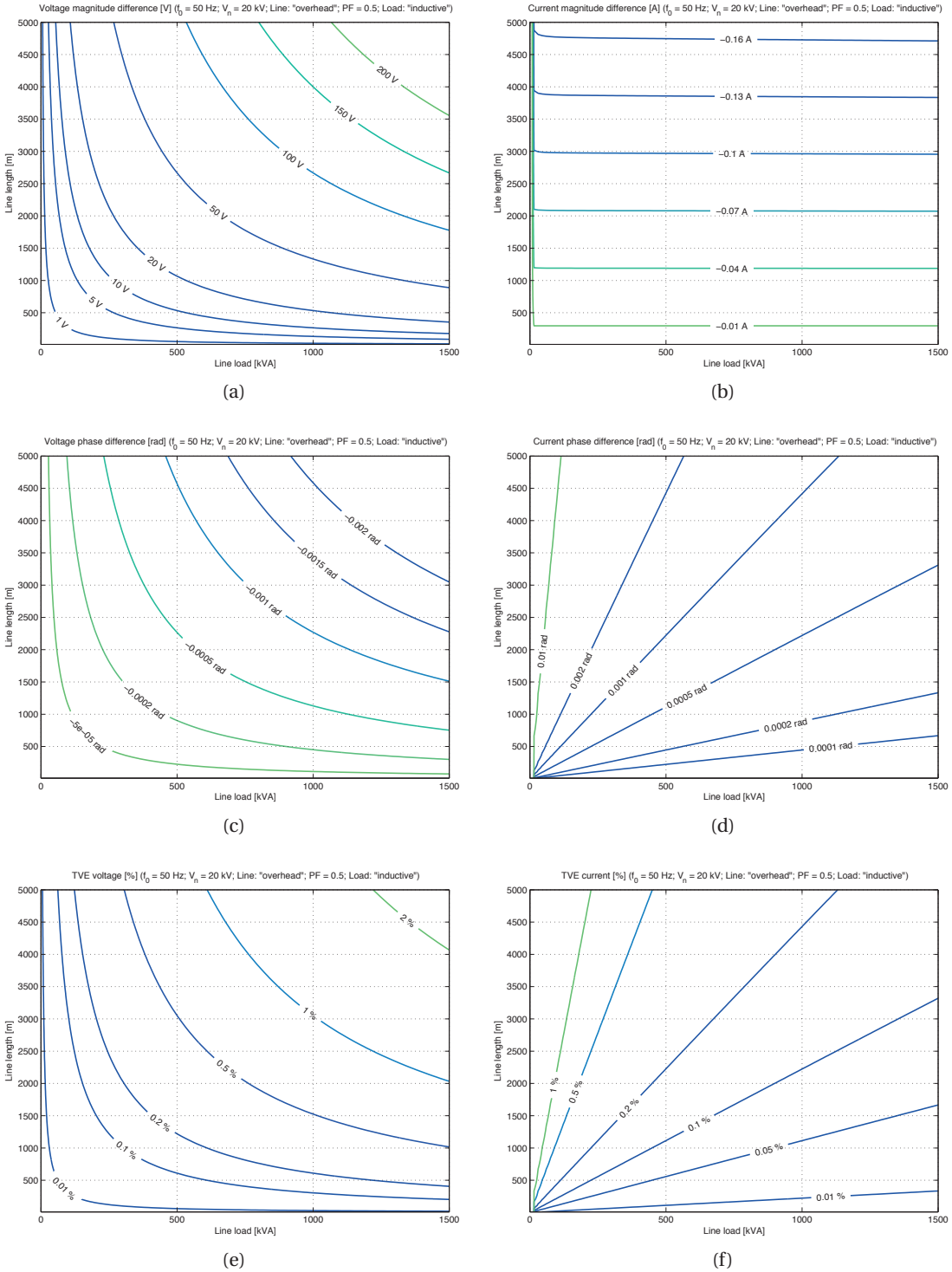


Figure 2.5 – Simulation results for an overhead line, nominal voltage $V_n = 20$ kV, power factor $\cos\varphi = 0.5$ showing the influence of the line load (x-axis) and line length (y-axis) on the amplitude (a,b) and phase differences (c,d) between voltage (a,c) and current (b,d) phasors measured at the beginning and at the end of a line. The related TVE requirements are derived in figures (e) and (f) for voltage and current phasors respectively.

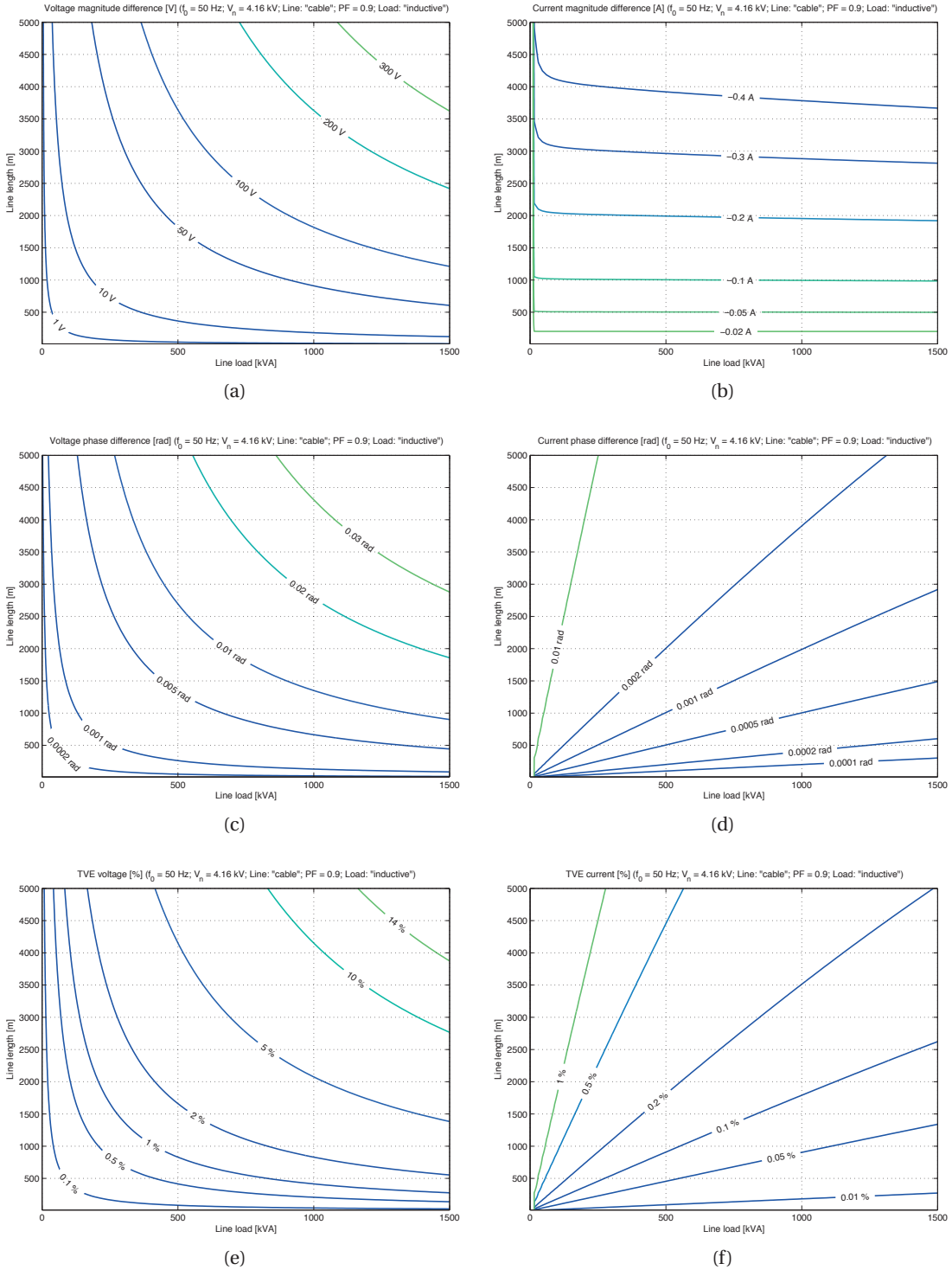


Figure 2.6 – Simulation results for a cable line, nominal voltage V_n = 4.16 kV, power factor $\cos\varphi$ = 0.9 showing the influence of the line load (x-axis) and line length (y-axis) on the amplitude (a,b) and phase differences (c,d) between voltage (a,c) and current (b,d) phasors measured at the beginning and at the end of a line. The related TVE requirements are derived in figures (e) and (f) for voltage and current phasors respectively.

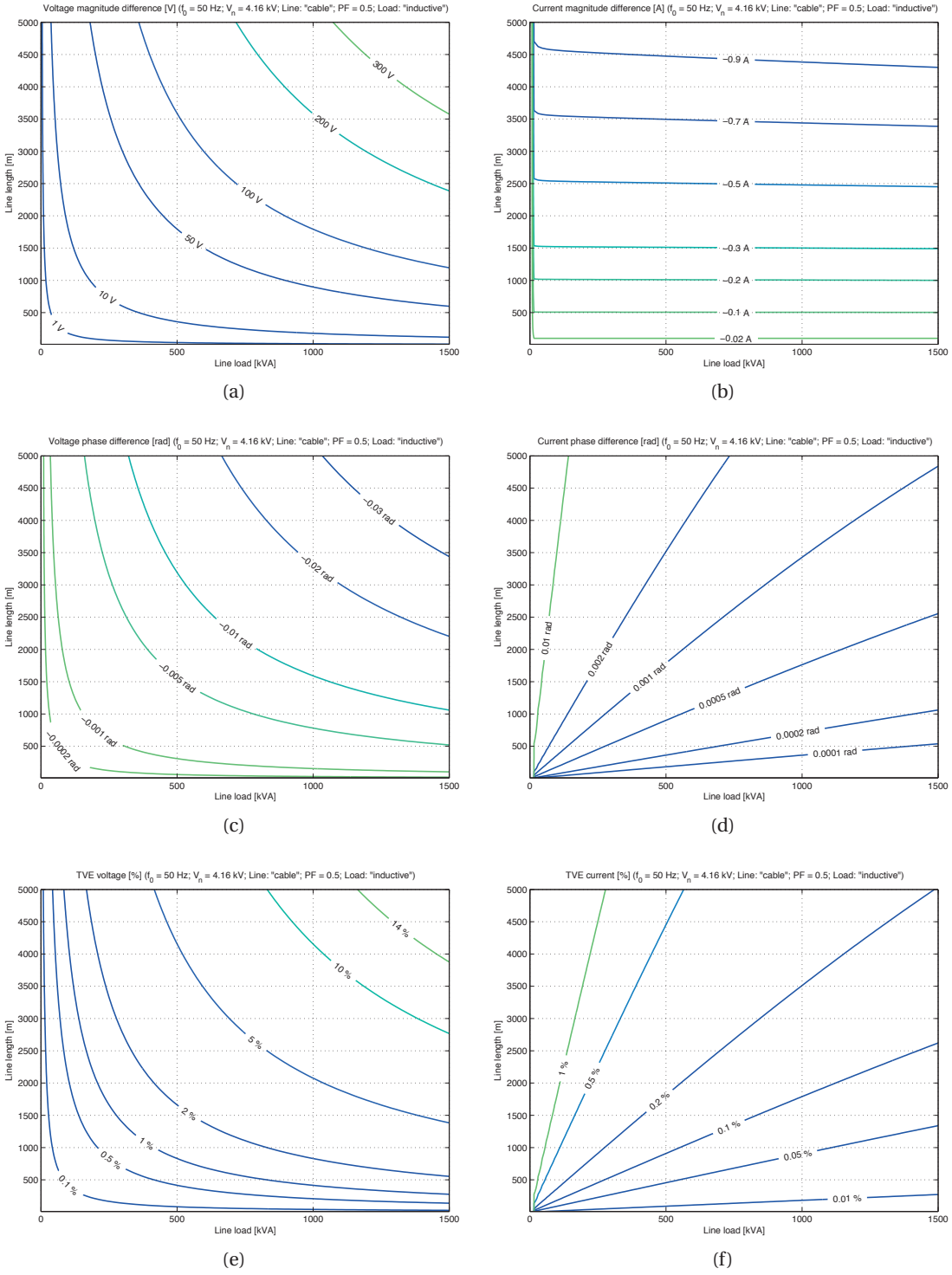


Figure 2.7 – Simulation results for a cable line, nominal voltage V_n = 4.16 kV, power factor $\cos\varphi$ = 0.5 showing the influence of the line load (x-axis) and line length (y-axis) on the amplitude (a,b) and phase differences (c,d) between voltage (a,c) and current (b,d) phasors measured at the beginning and at the end of a line. The related TVE requirements are derived in figures (e) and (f) for voltage and current phasors respectively.

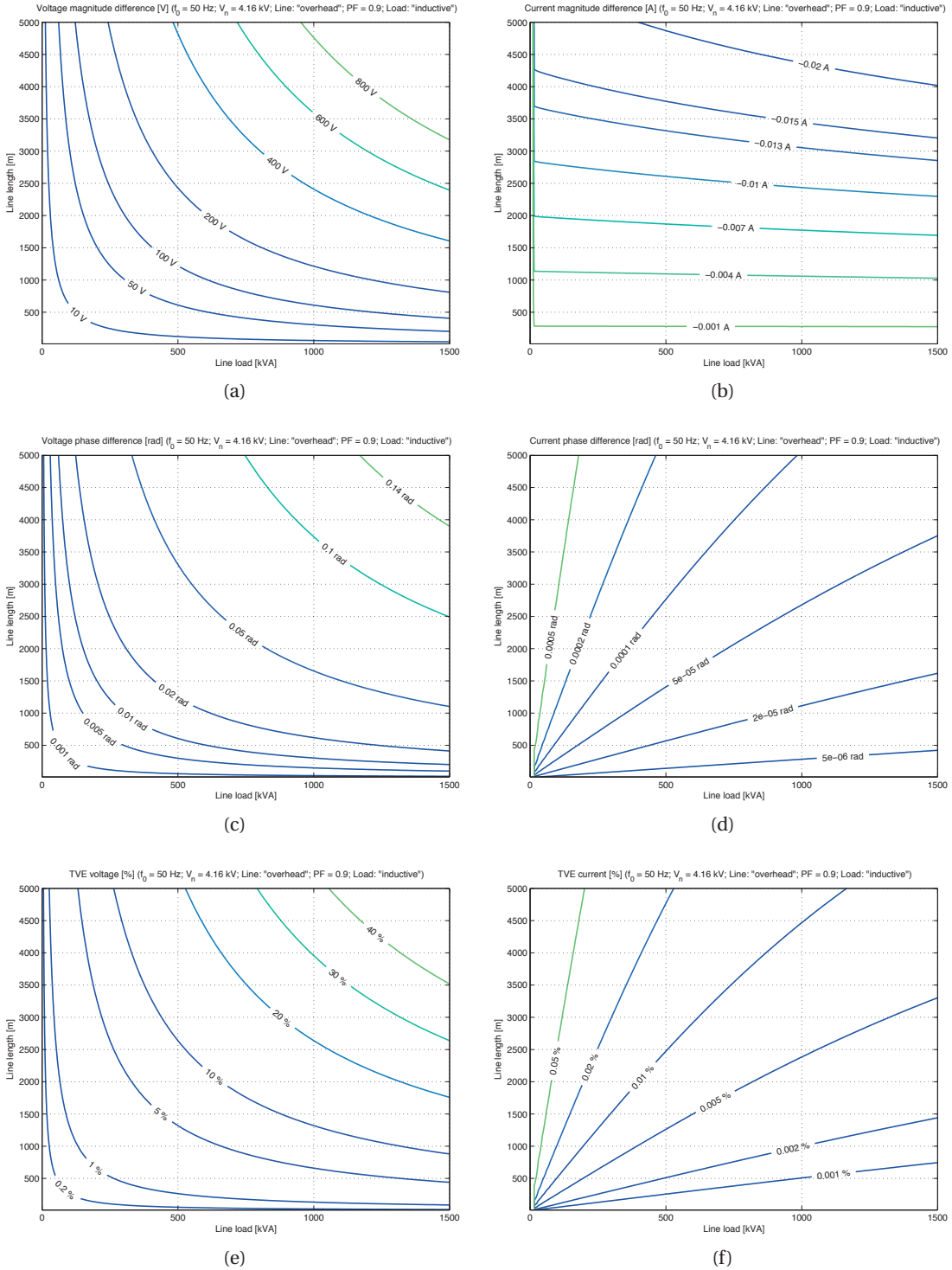


Figure 2.8 – Simulation results for an overhead line, nominal voltage V_n = 4.16 kV, power factor $\cos\varphi = 0.9$ showing the influence of the line load (x-axis) and line length (y-axis) on the amplitude (a,b) and phase differences (c,d) between voltage (a,c) and current (b,d) phasors measured at the beginning and at the end of a line. The related TVE requirements are derived in figures (e) and (f) for voltage and current phasors respectively.

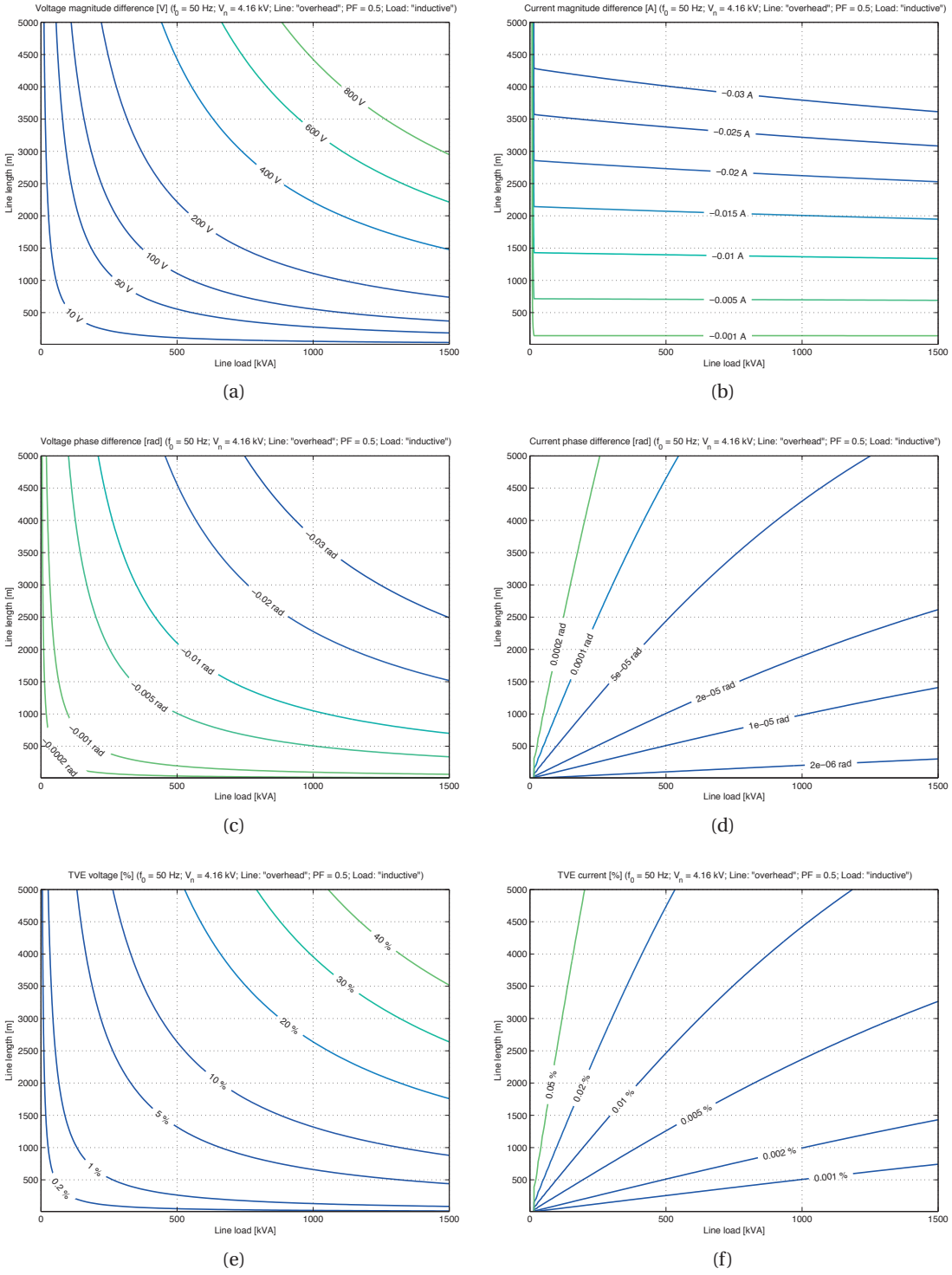


Figure 2.9 – Simulation results for an overhead line, nominal voltage V_n = 4.16 kV, power factor $\cos\varphi = 0.5$ showing the influence of the line load (x-axis) and line length (y-axis) on the amplitude (a,b) and phase differences (c,d) between voltage (a,c) and current (b,d) phasors measured at the beginning and at the end of a line. The related TVE requirements are derived in figures (e) and (f) for voltage and current phasors respectively.

3 Synchrophasor Estimation Based on the Iterative-Interpolated DFT technique

This chapter presents, formulates and validates in a simulation environment a novel synchrophasor estimation algorithm, hereafter referred as iterative-Interpolated DFT, to be deployed in PMUs expected to operate in ADNs. The algorithm, as it will be demonstrated next, considerably improves the accuracies of classical DFT- and IpDFT-based techniques and is capable to keep the same static and dynamic performances independently of the adopted window length that can be reduced down to 2 cycles of signal at the nominal frequency of the power system.

3.1 The Selection of the Synchrophasor Estimation Technique

The synchrophasor estimation algorithm is definitely the most relevant element of a PMU. Particularly in Active Distribution Networks (ADNs), the uncertainties introduced by the SE algorithm might overcome those introduced by the other components of a PMU (see Figure 1.3) due to the highly distorted waveforms that the SE algorithm needs to process.
When formulating a SE algorithm, one is naturally led to wonder whether a specific synchrophasor estimation technique is by definition better than others. A correct and definite answer does not exist and this is mainly due to the various metrics that can be used to define the quality of a synchrophasor estimation algorithm. In case more emphasis is put on the estimation accuracy in steady state and/or dynamic conditions, in case the focus is on the measurement reporting latencies and response times, or in case the computational complexity of the algorithm is a critical factor, different answers could be given to this question.
As a consequence, when building up a PMU, the selection of the SE technique is typically based on the personal expertise of the PMU developer and on the targeted power system application that will make use of the data produced by the PMUs installed in the field. If this is an offline post-processing of PMU data to identify inter-area oscillations or a real-time fault identification and location, the PMU requirements vary a lot and these differences are not described in any standard. Additionally, a key factor when selecting the SE technique

is related to the power system voltage level where the PMU will be installed. Whether the PMU will be installed and operate at transmission or distribution level, the SE algorithm requirements are quite different (see Chapter 2) and not every SE technique might be able to satisfy them. In particular as demonstrated in the previous Chapter, the lower the voltage level the more demanding the PMU requirements in terms of both rejection of harmonics and inter-harmonics, and in terms of capability to keep the same accuracy levels both during steady-state conditions and during power system transients.
In this respect in what follows the analysis will focus on the formulation of a synchrophasor estimation algorithm capable to be feasibly deployed into a PMU prototype that will operate in power distribution networks. Particularly, the proposed SE technique is a novel method based on the classical Discrete Fourier Transform theory. The origin of this choice can be partially found in the original background of this research but mainly it relies on some of the intrinsic qualities of this category of SE algorithms. Mainly we refer to: (i) the inherent DFT capability to isolate and identify the main tone of a discrete sinusoidal signal and to (ii) reject close-by harmonics; (iii) the relatively low computational complexity, particularly when the DFT spectrum is computed through one of the well known algorithms (e.g., Fast Fourier Transform – FFT [3] or Sliding DFT [78]). Nevertheless these qualities comes with non-negligible drawbacks and limitations that typically characterize the DFT: mainly they refer to the fact that the DFT theory assumes a periodic signal with time-invariant parameters, at least along the observation window. The latter, from one side should be as short as possible to be closer to the above-mentioned quasi steady-state hypothesis also during power system transient; on the other hand longer windows are needed when interested in rejecting and isolate harmonic and inter-harmonic signals that are quite frequent in ADNs (see Section 2.3).
This Chapter is structured as follows: Section 3.2 will recall the DFT formulation and illustrate the well known aliasing and spectral leakage effects. This section, although describing well known concepts in signal processing, serves to introduce the nomenclature that is used in the rest of the Chapter. Section 3.4 presents the formulation of the well known Interpolated DFT (IpDFT) algorithm and applies it to the estimation of synchrophasors. Then, Section 3.5 formulates a novel algorithm, called iterative-Interpolated DFT (i-IpDFT) that enhances the performances of standard IpDFT algorithms by iteratively compensating the effect of the spectral interference produced by the negative image of the spectrum. Finally Section 3.5.3 will demonstrate the qualities of the previously formulated SE algorithm by experimentally validating the effects of the proposed iterative technique in a simulation environment that implements some of the testing conditions dictated in the IEEE Standard [1].

3.2 The Discrete Fourier Transform

The Discrete Fourier Transform (DFT) is a numerical approximation of the theoretical Fourier Transform of a continuous and infinite duration signal. It represents the most common tool for engineers to extract the frequency content of a finite and discrete signal sequence, obtained from the periodic sampling of a continuous waveform in time domain (in the specific case of

PMUs, the sequence is obtained by periodic sampling of the voltage/current waveforms by means of A/D converters).
This Section derives the analytical formulation of the DFT starting from the theoretical formulation of the Fourier Transform of a continuous signal of infinite duration. Next it investigates the artificial effects caused by DFT and defines a synchrophasor estimation algorithm purely based on the calculation of the DFT to demonstrate its inaccuracies. Finally it focuses on the identification and analysis of the DFT parameters in order to be able to better select them when developing any DFT-based SE algorithm.

3.2.1 From the Fourier Transform to the Discrete Fourier Transform

The Fourier Transform of a continuous time-function $x(t)$, satisfying certain integrability constraints [79] is defined as follows:

$$X(\omega) = \int_{-\infty}^{+\infty} x(t) e^{-j\omega t} \mathrm{d}t. \tag{3.1}$$

being $\omega = 2\pi f$ the angular frequency[1]. In the field of continuous-time signal processing, (3.1) is used to transform a continuous time-domain function $x(t)$ to a continuous frequency-domain function $X(\omega)$. Nevertheless, in the field of digital signal processing (3.1) is nothing more than en elegant analytical tool that cannot be applied in the real world as continuous signals cannot be processed by any digital hardware and need first to be converted to a sequence of numbers by applying a periodic sampling process.
In this respect, the Discrete Time Fourier Transform (DTFT) has been defined to represent discrete sequences of infinite length in the frequency domain [3]:

$$X(\omega) = \sum_{n=-\infty}^{\infty} x(n) e^{-j\omega n}. \tag{3.2}$$

It consists of a transformation of a discrete sequence of infinite length $x(n)$ into a continuous frequency-domain function $X(\omega)$. Still such a transformation cannot be applied to the analysis of real signals, as it assumes the possibility to calculate an infinite summation that is in practice impossible.
Another way to represent an infinite sequence of samples in the frequency domain is by means of the so-called Discrete Fourier Series (DFS) that is nothing but a frequency-discretized version of the DTFT [3]:

$$\widetilde{X}(k) = \sum_{n=0}^{N-1} \tilde{x}(n) e^{-j\frac{2\pi kn}{N}}, \qquad 0 \le k \le N-1 \tag{3.3}$$

being $\tilde{x}(n)$ an infinite periodic sequence and N its period. Such a representation is feasible in practice, as it just involves the summation of N terms, but it assumes that the discrete

[1] Henceforth in the thesis, when discussing about the Fourier transform or the equivalent representation for discrete-time signals (DTFT), the ordinary frequency $X(f)$ or the angular frequency $X(\omega)$ notations will be interchangeably used.

sequence $\tilde{x}(n)$ is periodic with period N. In particular, the DFS differs from the DTFT in that its input and output sequences are both finite; it is therefore said to be the Fourier analysis of periodic discrete-time functions.
When the Discrete Fourier Series is used to represent a generic (i.e., not necessarily periodic) finite-length sequence of samples $x(n)$, $n \in [0, N-1]$, it is called the Discrete Fourier Transform (DFT) that is defined as follows:

$$X(k) \triangleq \frac{1}{B} \sum_{n=0}^{N-1} w(n)x(n)W_N^{kn}, \qquad 0 \leq k \leq N-1 \tag{3.4}$$

where $w(n)$ is a discrete windowing function that is used to extract a portion of the infinite length original sequence (see Section 3.2.4 for further details about windowing functions),

$$B \triangleq \sum_{n=0}^{N-1} w(n) \tag{3.5}$$

is the DFT normalization factor and

$$W_N \triangleq e^{-j2\pi/N} = \cos(2\pi/N) - j\sin(2\pi/N), \qquad W_N^{kN} = 1, k \in \mathbb{N} \tag{3.6}$$

is the so called *twiddle factor*.
The DFT spectrum can be equivalently expressed in matrix form for a more intuitive understanding of its logic:

$$\begin{bmatrix} X(0) \\ X(1) \\ \vdots \\ X(k) \\ \vdots \\ X(N-1) \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & \dots & 1 \\ 1 & W_N & W_N^2 & \dots & W_N^{N-1} \\ \vdots & \vdots & \vdots & & \vdots \\ 1 & W_N^{(k)_N} & W_N^{(2k)_N} & \dots & W_N^{((N-1)k)_N} \\ \vdots & \vdots & \vdots & & \vdots \\ 1 & W_N^{N-1} & W_N^{N-2} & \dots & W_N \end{bmatrix} \begin{bmatrix} x(0) \\ x(1) \\ \vdots \\ x(k) \\ \vdots \\ x(N-1) \end{bmatrix} \tag{3.7}$$

where $(\cdot)_N$ identifies the $\bmod N$ operator.

3.2.2 DFT Interpretation and Relevant Properties

The DFT is a sequence of complex values that are equally spaced in the frequency spectrum and represent, under specific conditions, a portion of the Fourier Transform of the original continuous signal $x(t)$ (see Section 3.2.3 for further details about the original assumptions to guar antee an exact matching between the DFT and the Fourier Transform). It is the result of a frequency decomposition of the finite-length discrete signal that is projected onto the sinusoidal basis set W_N^{kn}, $0 \leq k \leq N-1$.
In order to correctly interpret the DFT spectrum obtained by applying equation (3.4) to a generic real-valued finite sequence $x(n)$, some considerations must be made.

DFT Periodicity

As shown in Section 3.2, the DFT of a finite sequence of real values $x(n)$ is a finite sequence of complex values $X(k)$ (also called "bins") defined in the interval $0 \leq k \leq N-1$. This does not mean that the DFT cannot be computed outside of the interval $0 \leq k \leq N-1$, but simply that this will result into a periodic extension of $X(k)$, due to the periodicity of the theoretical spectrum of the sampled signal.
Usually, when analyzing signals through the DFT, the convention is to associate the DFT bins in the interval $0 \leq k \leq N/2-1$ to the positive frequencies and the bins in the interval $N/2 \leq k \leq N-1$ to the "negative" frequency range.

DFT Frequency Axis Discretization

The k-th DFT bin represents the frequency content of the original signal at the normalized frequency $2\pi k/N$ as it is the result of the projection of the finite-length sequence into the basis vector characterized by that frequency (see equation (3.4)). As a consequence, consecutive bins are separated by the normalized frequency interval $2\pi/N$ and the whole DFT spectrum will cover the normalized frequency interval $[0, 2\pi]$. Nevertheless such a scale is not always practical as it is not associate to any physical quantity.
In order to derive a more practical scale for the DFT frequency axis, it should not be forgotten that the finite-length sequence $x(n)$ is associated to specific instants in time according to the adopted sampling rate F_s. Therefore, based on the sampling rate, the window length can be expressed as a function of time as $T = N/F_s$ and, accordingly, each basis vector W_N^{kn} can be referred to an absolute frequency. In particular, the bin for $k = 0$ can be associated to the DC component ($f = 0$), the bin for $k = 1$ to a frequency $f = 1/T$ and a generic k-th bin to a frequency $f = k/T$. It is then clear that the frequency separation between two consecutive bins is $\Delta f = 1/T$ and can only be increased at the price of enlarging the window length T. On the other hand, the frequency range that can be represented with the DFT of the finite-length sequence $x(n)$ obtained by sampling the original signal $x(t)$ with a sampling rate F_s is $[-F_s/2, F_s/2]$.

DFT Symmetry

The DFT of a real-valued sequence is symmetric. In particular, the DFT bins in the interval $0 \leq k \leq N/2-1$ (positive frequency range) are related to those in the interval $N/2 \leq k \leq N-1$[2]

[2] Or, equivalently, due to the DFT periodicity, in the interval $-N/2 \leq k \leq -1$.

(negative frequency range) based on the following equivalences:

$$\begin{cases} X(k) = X^*((k)_N) \\ \mathrm{Re}(X(k)) = \mathrm{Re}(X((-k)_N)) \\ \mathrm{Im}(X(k)) = -\mathrm{Im}(X((-k)_N)) \\ |X(k)| = |X((-k)_N)| \\ \angle X(k) = -\angle X((-k)_N) \end{cases} \tag{3.8}$$

As a consequence, when applying the DFT to real-valued signals, each frequency component will appear twice in the DFT spectrum: once in the positive frequency range (the so called *positive image*) and once in the negative frequency range (the so-called *negative image*)

3.2.3 DFT Effects

As demonstrated in the previous Section, the DFT is a sampled version of a portion of the DTFT of the sampled signal. On the other hand the DFT is often improperly considered as a "sampled" version of the continuous Fourier Transform. This statement is partially correct and the two transformations can be considered equivalent only if both of the following assumptions are respected:

- the original signal can be perfectly reconstructed from the discrete sequence of samples;
- the original signal is periodic and characterized by a period that is contained an integer number of times in the adopted window length.

In general this is not always the case and, as we will see next, the DFT is only the approximation of the continuous Fourier Transform and its correct interpretation derives only from the perfect knowledge of the DFT theoretical background.
In order to understand the above mentioned assumption we could make reference to Figure 3.1, where the basic steps to apply the DFT to a continuous-time signal $x(t)$ representing a generic physical phenomenon are shown. The original continuous signal needs first to be transformed to an equivalent sequence of samples $x(n)$. This, in the real world, is typically performed by an A/D converter that, for the time being, is considered to be ideal; in other words it is assumed to produce a sequence of equally-spaced samples that are equal to the original signal evaluated at regular time intervals $x(n) = x(nT_s)$, being $T_s = 1/F_s$ the sampling time. The A/D conversion process produces an infinite sequence of samples that, in order to be processed by the DFT, needs to be sectioned in portions containing the same number of samples N. This is done by applying to the infinite sequence $x(n)$ a finite duration windowing function $w(n)$ that, for the sake of simplicity, will be represented by a rectangular function that is 1 inside of the interval $0 \leq n \leq N-1$ and 0 elsewhere. After this steps the DFT can be applied to each portion of the sampled signal.
In what follows, each one of the above-mentioned steps is analytically modeled and analyzed

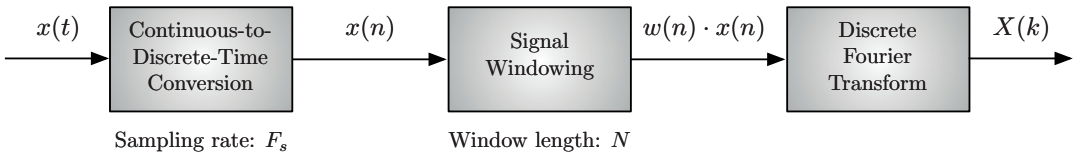


Figure 3.1 – Main steps when applying a DFT-based digital signal processing technique to a continuous signal $x(t)$.

using the Fourier Transform theory. This will help understanding the previously mentioned assumptions and derive the 2 main DFT error sources, namely *aliasing* and *spectral leakage*.

Aliasing

The sampling process can be modeled as the multiplication of the input continuous signal $x(t)$ with a periodic impulse train $s(t)$:

$$x_s(t) = x(n \cdot T_s) = x(t) \cdot s(t) \tag{3.9}$$

$$= x(t) \cdot \sum_{n=-\infty}^{\infty} \delta(t - nT_s) \tag{3.10}$$

$$= \sum_{n=-\infty}^{\infty} x(nT_s) \cdot \delta(t - nT_s) \tag{3.11}$$

being δ the unit impulse function, or Dirac delta function (see Figure 3.2).
The frequency domain representation of this transformation can be given by applying the Fourier Transform theory and properties to equation (3.10). In particular, by recalling that the Fourier Transform of the product of two functions is the convolution of the Fourier Transforms of the two functions, the Fourier Transform of the sampled signal can be analytically derived as follows:

$$x_s(t) = x(t) \cdot \sum_{n=-\infty}^{\infty} \delta(t - nT_s) \quad \overset{\mathfrak{F}}{\rightarrow} \quad X_s(f) = X(f) * \frac{1}{Ts} \sum_{k=-\infty}^{\infty} \delta\left(f - \frac{k}{T_s}\right) \tag{3.12}$$

$$= \frac{1}{T_s} \sum_{n=-\infty}^{\infty} X\left(f - \frac{k}{T_s}\right) \tag{3.13}$$

where, to obtain equation (3.13), we have taken advantage of the property that the convolution between a Dirac δ function and any generic function is the value of the generic function evaluated at the location of the Dirac δ function.
As a consequence the Fourier Transform of the sampled signal is composed by infinite copies of the spectrum $X(f)$ of the original continuous signal $x(t)$ that are shifted by integer multiples of the sampling frequency $F_s = 1/T_s$ and then superimposed, to produce the periodic Fourier Transform depicted in Figure 3.3 for a band-limited original spectrum characterized by a bandwidth Ω_N and a sampling rate $\Omega_s = 2\pi F_s$.
From Figure 3.3 it is obvious to verify that, if the signal is band-limited with bandwidth

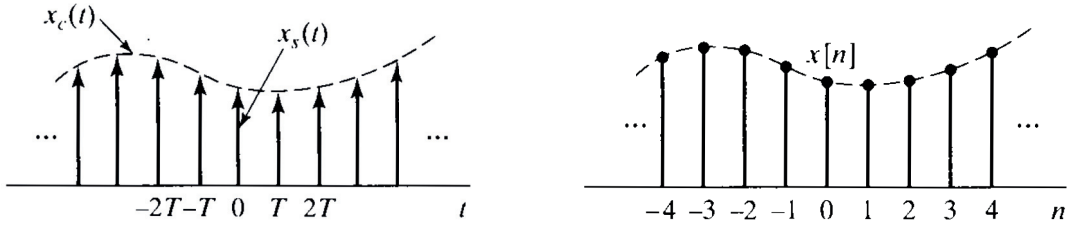


Figure 3.2 – The sampling process modeled as the multiplication of the original signal with a periodic impulse train (adapted from [3]).

$\Omega_N < \Omega_s/2$, the spectrum copies are not overlapping and the original spectrum $X(f)$ can be reconstructed by low-pass filtering the base-band copy of the spectrum $X_s(f)$. On the other hand, if this is not the case and the bandwidth of the original signal is higher than half of the sampling rate F_s ($\Omega_N > \Omega_s/2$), the spectrum copies are overlapping so that when they add together, the original spectrum $X(f)$ is no longer recoverable by low-pass filtering.
The latter phenomenon is called *aliasing* and it results into a distortion of the original signal that cannot be any longer be reconstructed from the sampled signal. Such a phenomenon is the basis of the well-known Nyquist-Shannon sampling theorem [3]:

Theorem. *Let $x(t)$ be a band-limited signal and $X(f)$ its Fourier Transform with*

$$X(f) = 0, \qquad f > \frac{\Omega_N}{2\pi}.$$

Let $x(n) = x(nT_s), n \in \mathbb{N}$ be an infinite sequence of equally spaced samples obtained by sampling the continuous signal $x(t)$ with a sampling frequency $F_s = 1/T_s$.
Then $x(t)$ is uniquely determined by the sequence of samples $x(n) = x(nT_s)$ if

$$F_s > \Omega_N/\pi$$

In other words, in order to be able to correctly reconstruct the signal $x(t)$ from the infinite sequence of samples $x(n)$, the original signal must be sampled at a sampling rate F_s that must be at least two times higher than the maximum frequency component contained in the original spectrum $X(f)$.

Spectral Leakage

Once the original continuous signal $x(t)$ has been sampled, it must be sectioned in portions to be analyzed by the DFT. This process is called windowing and it consists in multiplying the infinite sequence of samples $x(n)$ by a specific windowing function (see Figure 3.4).
For the sake of simplicity (nevertheless, such an analysis can be easily extended to any type of signal) we will now assume that the input signal is dominated by a sinusoidal component at

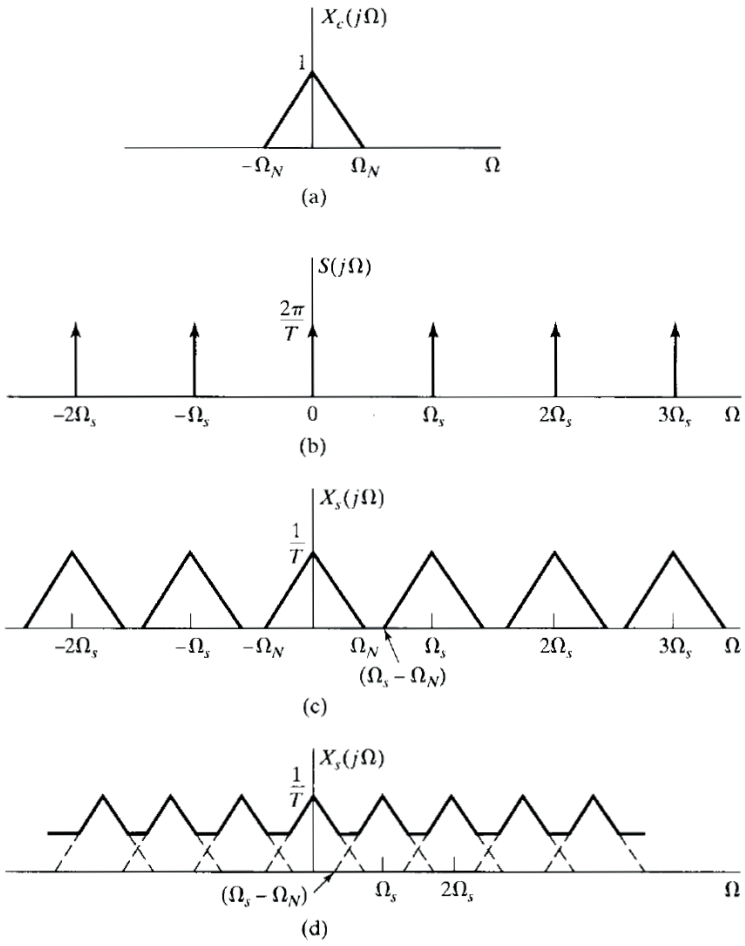


Figure 3.3 – The effects of aliasing for a signal characterized by a bandwidth Ω_N and sampled at a frequency $\Omega_s = 2\pi F_s$ (adapted from [3]). The Fourier Transforms of the original signal (a), of the impulse train (b) and of the sampled signal with a sampling rate respecting (c) or violating (d) the Nyquist-Shannon theorem are shown.

the nominal frequency of the power system:

$$x(t) = A\cos(2\pi f_0 t) \tag{3.14}$$

that is characterized by a Fourier Transform

$$X(f) = \frac{A}{2}\left[\delta(f - f_0) + \delta(f + f_0)\right]. \tag{3.15}$$

The windowing operation can then be modeled as the multiplication between the sampled sinusoidal signal $x_s(t)$ and the rectangular window function $w_r(t)$:

$$x_{s,w}(t) = w_r(t) \cdot x_s(t) = w_r(t) \cdot [x(t) \cdot s(t)] \tag{3.16}$$

$$= [w_r(t) \cdot x(t)] \cdot s(t) \tag{3.17}$$

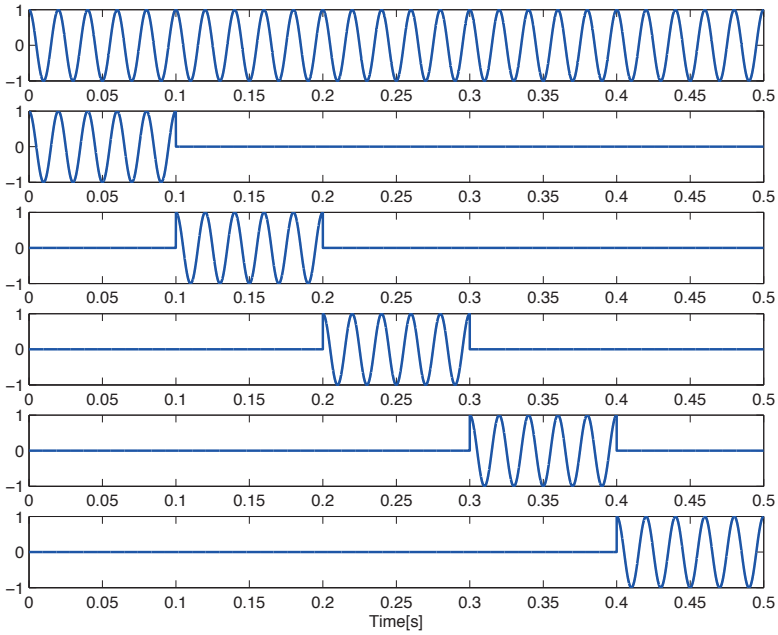


Figure 3.4 – Successive applications of a rectangular window function to an original infinite sequence $x(n)$ to be able to apply the DFT.

$$= \left[w_r(t) \cdot A\cos(2\pi f_0 t) \right] \cdot \sum_{n=-\infty}^{\infty} \delta(t - nT_s) \tag{3.18}$$

By recalling that the Fourier Transform of the product between two functions equals the convolution between the Fourier Transform of each one of the two functions

$$x_w(t) = x(t) \cdot w_r(t) \xrightarrow{\mathfrak{F}} X_w(f) = W_r(f) * X(f) \tag{3.19}$$

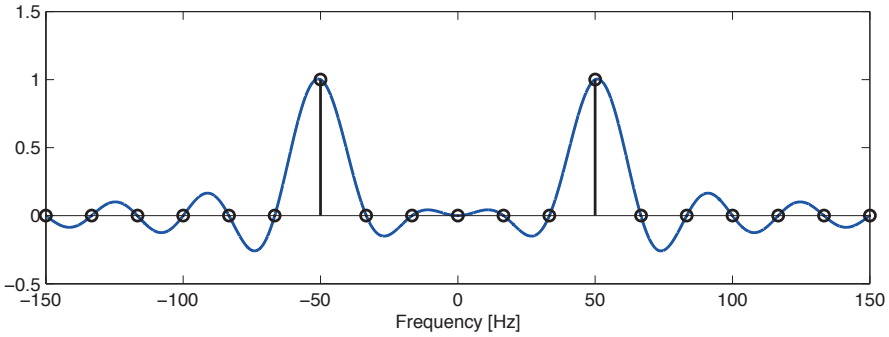
and that the convolution between a Dirac δ function and any generic function is the value of the generic function evaluated at the location of the Dirac δ function, the Fourier Transform of $x_{s,w}(t)$ can be computed as:

$$x_{s,w}(t) \xrightarrow{\mathfrak{F}} X_{s,w}(f) = \left[W_r(f) * X(f) \right] * S(f) \tag{3.20}$$

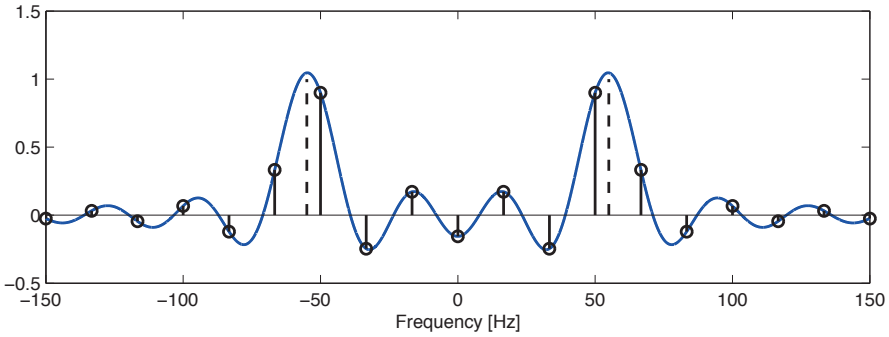
$$= \frac{A}{2} \left[W_r(f - f_0) + W_r(f + f_0) \right] * \frac{1}{T_s} \sum_{k=-\infty}^{\infty} \delta\left(f - \frac{k}{T_s} \right) \tag{3.21}$$

$$= \frac{A}{2T_s} \sum_{n=-\infty}^{\infty} \left[W_r\left(f - \frac{k}{T_s} - f_0 \right) + W_r\left(f - \frac{k}{T_s} - f_0 \right) \right] \tag{3.22}$$

In other words, the spectrum of the sampled and windowed signal $x_{s,w}(t)$ is composed by infinite copies of the spectrum of the windowed signal $W_r(f) * X(f)$ shifted by integer multiples of the sampling rate $F_s = 1/T_s$ and then superimposed.
In order to illustrate the effects of leakage on the DFT, let's consider just the base-band copy of the spectrum of $X_{s,w}(f)$ (i.e., for $k = 0$). Additionally, let's adopt the simplest windowing



(a)



(b)

Figure 3.5 – The DTFT (in blue) and the DFT (in black) of a sinusoidal signal windowed with a rectangular window of length $T = 60$ ms and characterized by a nominal frequency of 50 (a) and 55 (b) Hz respectively. In (a) the effects of leakage are not visible since the adopted window contains an integer number of periods of the input signal; they appear in (b) where the adopted window length is not a multiple of the period of the input signal.

function, namely the rectangular one[3].
As recalled in Appendix A.1, the Fourier Transform of a rectangular window is correctly represented with a sinc function (see Figure A.1)

$$\text{sinc}(fT) = \frac{\sin(\pi fT)}{\pi fT} \tag{3.23}$$

that is characterized by a peculiar property:

$$\text{sinc}(fT)\big|_{f=\frac{1}{T}} = 0 \tag{3.24}$$

namely the zero-crossing of the Fourier Transform of the rectangular window are equally spaced and happens at integer multiples of $1/T$.
According to equation (3.22), the base-band copy of the Fourier Transform of $X_{s,w}(f)$ will be composed by two sinc functions centered around $\pm f_0$. In case f_0 is a multiple of the DFT

[3]Nevertheless such an analysis can be made with any other kind of window (see Section 3.2.4 for further details about the various type of windowing functions).

frequency resolution $\Delta f = 1/T$ (i.e., if the window contains an integer number of periods of the signal), the zero crossings of the translated sinc functions happen exactly at multiples of $1/T$. The only frequency that will have a non-zero projection into the DFT basis set will be $f = \pm f_0$ (i.e., the DFT bin with index $k = f_0/\Delta f$) and the resulting DFT will be characterized by only two non-zero bins, at index $\pm k$ (see Figure 3.5a).
On the other hand, if f_0 is not a multiple of the frequency resolution Δf (i.e., if the window does not contain an integer number of periods of the signal), the zero crossings of the translated sinc functions, do not happen exactly at multiples of $1/T$. Therefore all the discrete frequencies will exhibit non-zero projections on the DFT basis set even though the majority of the spectrum energy will still be concentrated around $f = f_0$ (see Figure 3.5b).
This effect is the so-called *spectral leakage* and it arises when the sampling process is not synchronized with the fundamental tone of the signal under analysis and the DFT is computed over a non-integer number of cycles of the input signal. As it will be discussed later, spectral leakage can be separated into *short-term* and *long-term* spectral leakage: the first refers to the effects of the main lobe width of the Fourier Transform of the adopted window that can cause difficulties in identifying the "true" maximum of a specific portion of the DFT spectrum. The latter, on the other hand, refers to the effect caused by the side-lobes (i.e., the "tails") of the Fourier Transform of the adopted window that can generate the so-called spectral interference between nearby tones.

Spectral Sampling

As previously mentioned, the DFT of the sequence $x(n)$, $n \in [0, N-1]$, provides samples of the DTFT of the equivalent windowed signal, at N, equally spaced discrete frequencies $f_k = k \cdot \Delta f = k/T$, being $-N/2 \leq k \leq N/2-1$ (see Figure 3.5). Consequently the location of the discrete frequencies and consequently the "shape" of the DFT changes based on the adopted number of samples N and window length T.
In general, when the target is identifying the parameters of a signal, the frequency resolution Δf plays a major role as it defines the accuracy in locating the correct position in the frequency spectrum of the tone under analysis. As we will see later, the IpDFT method will partially overcome such a limitation with a proper interpolation of the DFT bins.

3.2.4 The DFT Parameters

The DFT output can be modified by acting on three main parameters: the sampling rate F_s, the window length T and the the window profile $w(n)$. They basically determine the aliasing and spectral leakage effects together with the discretization of the frequency axis. In what follows, each one of them will be carefully analyzed.

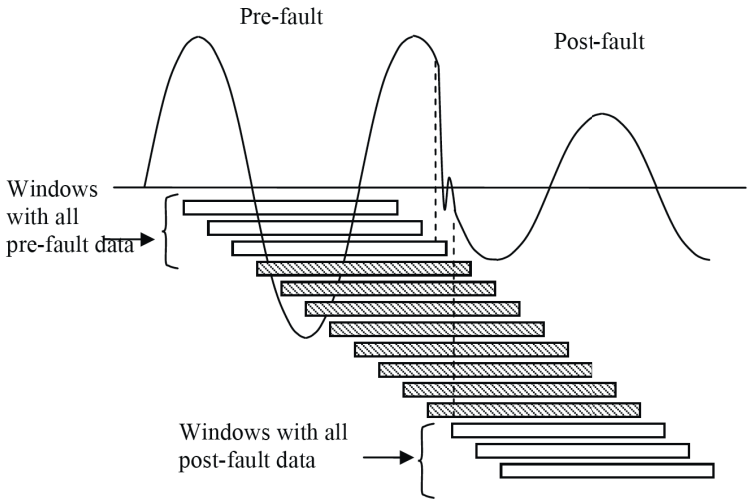


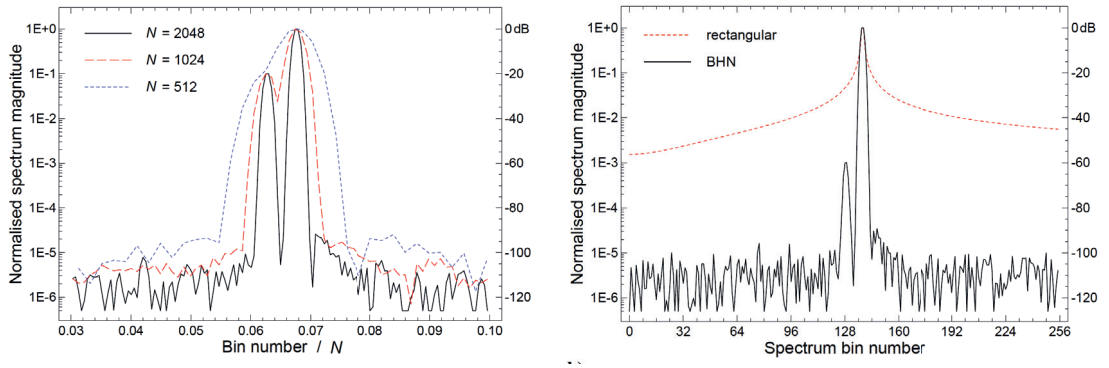
Figure 3.6 – The effects of the window length during a power-system fault. The window length affects the PMU response times and therefore the quality of the PMU estimations before and after the fault event (adapted from [4]).

The Sampling Rate

The sampling rate F_s defines the frequency range that can be correctly analyzed with the DFT. It is limited from one side by the Nyquist frequency (see Section 3.2.3) that can only be defined if the characteristics of the acquired signals are known; form the other side by the hardware limitations of the platform where the DFT will be deployed. Whereas in a simulation environment any sampling rate can be adopted, in the real world F_s is limited by the maximum and possible sampling rates of the adopted A/D conversion technology and by the processing and data storage capabilities of the processing unit (the higher the sampling rate the higher the amount of samples to be processed in real-time by the DFT).

The Window Length

Once the sampling rate has been fixed, the window length T defines both the number of samples $N = T/F_s$ to be processed and the frequency resolution $\Delta f = 1/T$ of the DFT. As mentioned before, the latter, is directly related to the uncertainty in correctly identifying the parameters of an input signal directly from the DFT output. On the other hand, the number of samples is an important parameter when processing waveforms corrupted by white noise. As shown in [4] the effects of white noise on the DFT uncertainty can be properly reduced by averaging, increasing the number of samples to be processed.
Additionally, the window length T is a quite important parameter when interested in identifying a tone that might be surrounded by other frequency components. Indeed the window length T influences the frequency separation between the zero-crossings of the sinc function (see Appendix A.1) and consequently the main lobe width and the way the side-lobes of any



(a) (b)

Figure 3.7 – The influence of spectral leakage on tone detectability: Figure (a) shows the influence of different window lengths N when a rectangular window is adopted, whereas Figure (b) the influence of different window profiles with a fixed window length $N = 2048$ (adapted from [5], BHN stands for the Blackman-Harris-Nuttal window, one of the window profiles with the lowest side-lobe levels).

windowing function decay. This in turn determines the tone detectability and the amount of spectral interference produced by near-by tones. In general, the higher the window length, the lower the effects of the spectral interference produced by near-by tones (see Figure 3.7a). Nevertheless the higher the window length the more probable the possibility that the waveform parameters within the window length are not constant at that therefore the DFT assumptions are not respected, introducing therefore an inherent error in the DFT spectrum.
Last but not least the window length T is a crucial parameter when applying the DFT to synchrophasor estimation. As reviewed in 1.3.3, the response times and measurement reporting latencies are two very important characteristics of a PMU that are mainly influenced by the adopted window length. In general, the lower the window length, the lower the response time and measurement reporting latencies and therefore the higher the possibility to use the PMU for specific applications that require fast response and reduced latencies (e.g., power system protections). This concept is depicted in Figure 3.6 in case of a power-system fault.

The Window Profile

In Section 3.2.3 it has been shown that spectral leakage arises when the input signal is not periodic within the window length. This has been demonstrated in the case of a rectangular window function but the proposed analysis could be extended to any kind of window.
As shown in [56] the characteristics of a window function can be expressed in terms of several figures of merit. For our purposes we can restrict the analysis to:

- the *main lobe width*, namely the width of the highest lobe of the adopted window (see Figure 3.5 in the case of a rectangular window), that is typically measured by evaluating

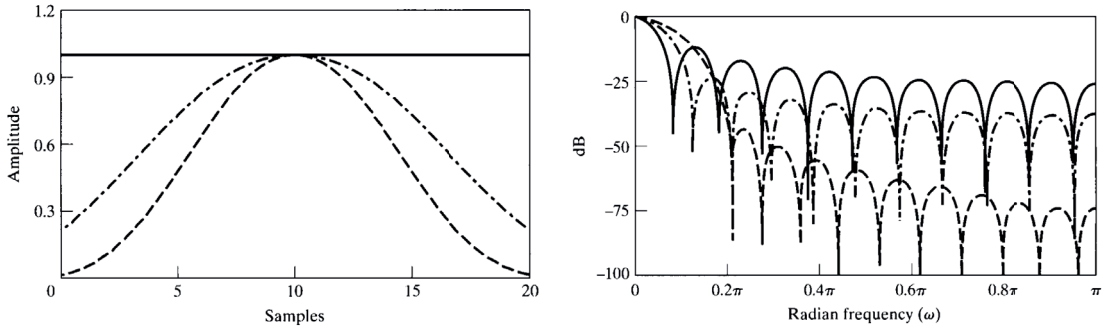


Figure 3.8 – The comparison of the time (a) and frequency (b) profiles of three different windowing functions (adapted from [3]): the rectangular window (continuous line), the Hanning window (dashed line) and the Hamming window (dash-dot line).

the 3 dB bandwidth of the Fourier Transform of the adopted window;

- the *side-lobe levels* and *decaying rate*, namely the relative height of the 2nd, 3rd, etc. lobes with respect to the height of the main one and their characteristic decaying rate.

Whereas both parameters impact the tone detectability, namely the capability to detect two nearby tones through DFT, the latter is also responsible of the already-mentioned spectral interference, namely the detrimental effect that neighboring tones produce on the main tone under analysis. This effect is quite noticeable when using a rectangular window (see Figure 3.5) that, besides being the windowing function with the minimum main lobe width, it is characterized by the highest side-lobes (see [56] for a detailed analysis of the window parameters). To improve this characteristic Harris in [56] has first defined various bell-shaped windowing functions that, by reducing the discontinuities at the edge of a window, reduce the side-lobe levels. Unfortunately this comes at the price of enlarging the main lobe width and therefore reducing the tone detectability (see Figure 3.8 for a time and frequency representation of the rectangular and 2 different bell-shaped windows).
In what follows, the analysis will focus on a specific window type that is the Hanning (or Hann) window. Such a window is defined as:

$$w_H(n) = \frac{1-\cos(2\pi n/N)}{2}, \quad n \in [0, N-1] \tag{3.25}$$

and its Fourier Transform is

$$W_H(\omega) = -0.25 \cdot D_N(\omega - 2\pi/N) + 0.5 \cdot D_N(\omega) - 0.25 \cdot D_N(\omega + 2\pi/N) \tag{3.26}$$

being $D_N(\omega)$ the Dirichlet kernel

$$D_N(\omega) = e^{-j\omega(N-1)/2} \frac{\sin(\omega N/2)}{\sin(\omega/2)} \tag{3.27}$$

also known as the generalized Fourier Transform of the rectangular window.
The Hanning window is characterized by a wider (almost double) main lobe width compared to the rectangular window but by lower side-lobes reducing therefore the eventual spectral interference between neighboring tones.

3.2.5 A Trivial DFT-based Synchrophasor Estimation Algorithm

For sake of comparison, it is interesting to formulate a SE algorithm barely based on the computation of the DFT spectrum. Although such an approach will suffer from reduced accuracies due to the above-mentioned DFT effects (see Section 3.2.3), a preliminary formulation of a DFT-based SE algorithm will help the reader in understanding the basic concepts related to "synchrophasor estimation" and the reasons behind the research of methods capable of reducing the detrimental effects of aliasing, spectral leakage and spectral sampling.
As known, the main task of a synchrophasor estimation algorithm is to assess the parameters of the fundamental tone of a signal by using a previously acquired set of samples representing a portion of an acquired waveform (i.e., node voltage and/or branch/nodal current).
A trivial approach to estimate the parameters of the main DFT tone might be based on the estimation of the position of a local DFT maximum within a specific frequency range. The related pseudo-code is shown below:

Algorithm 1 A trivial DFT-based synchrophasor estimation algorithm.

1: **procedure** TRIVIAL-SE($x(t)$)
2: sample the input signal $x(t)$ with sampling rate F_s to obtain the sequence $x(n)$;
3: apply the rectangular window $w_r(n)$ to $x(n)$;
4: compute the DFT of $w_r(n) \cdot x(n)$;
5: apply a maximum search technique to find the DFT bin with the highest amplitude $|X(k_m)|$;
6: **return** the amplitude, phase and frequency of $X(k_m)$;
7: **end procedure**

According to this method, the synchrophasor may be computed as:

$$\begin{cases} \widehat{f} = k_m \Delta f \\ \widehat{A} = |X(k_m)| \\ \widehat{\psi} = \angle X(k_m) \end{cases} \tag{3.28}$$

being k_m the index of the highest DFT bin of the spectrum.
The accuracy of this trivial synchrophasor estimator is related to the degree of correspondence between the "true" position of the main tone and the DFT maximum location (i.e. to the intensity of spectral leakage). The maximum error in the peak location is equal to half of the DFT frequency resolution $\Delta f = 1/T$, as the main spectrum tone may lie somewhere between the highest and 2$^{\text{nd}}$ highest bin of the DFT spectrum (see Figure 3.5b).

In particular it should be noticed that the relative error in the frequency estimation

$$\max(\epsilon_{f,\text{rel}}) = \frac{\max(\epsilon_f)}{f} = \frac{\max\left|k_m\Delta f - f\right|}{f} = \frac{1}{2}\frac{\Delta f}{f} = \frac{1}{2}\frac{F_s}{Nf} \tag{3.29}$$

is maximized when $F_s \gg f$, i.e., for frequency components lying in the beginning of the signal spectrum that is the case of typical spectrum analyzed by synchrophasor estimation algorithms.
The only possibility to improve the accuracy of this trivial synchrophasor estimation algorithm is to increase the frequency resolution Δf. In this respect there are two options, namely:

- decrease the sampling rate F_s (see equation (3.29)) with the undesirable possibility that aliasing may arise (see Section 3.2.3);
- increase the window length T and at the same time the number of sample to be processed N, introducing non-negligible errors in the computed DFT spectrum when dynamic conditions arise (see Section 3.2.4).

It turns out that both approaches are unpractical and particularly, in order to reach acceptable accuracy levels in the synchrophasor estimation by increasing T, the window length must be extended to values that are unacceptable in the field of synchrophasor estimation, especially with respect to the response time limits defined in Table 1.4.
In Section 3.4 a more elegant technique to overcome the limitations due to the DFT effects of spectral sampling and leakage will be presented.

3.3 DFT Calculation in Real-time

If not properly designed and implemented, the DFT calculation in real-time might represent a considerable bottleneck when developing a DFT-based synchrophasor estimation algorithm, in terms of both measurement reporting latencies and achievable reporting rates (see Section 1.3.3). Indeed, particularly when the DFT is calculated over a discrete sequence of samples obtained with a sampling rate of some tens of kHz, the high number of samples within a single observation window makes the DFT calculation according to equation (3.4) computationally intensive. This, combined with the maximum reporting rate and measurement latency requirements defined in [1], makes the development of a PMU based on the DFT, a quite challenging task.
In this respect, in order to improve both latencies and throughput, several efficient techniques to compute the DFT spectrum has been proposed in literature. These can be separated into two main categories: *recursive* and *non-recursive* algorithms.
Within the group of non-recursive algorithms the well known *Fast Fourier Transform* (FFT) algorithm (e.g., [80]) is widely used. Typically, this implementation is adopted to perform harmonic analysis over an extended portion of the spectrum even though its deployment on embedded system is usually onerous. When, on the other hand, only a subset of the overall

Table 3.1 – The computational complexity of the STFT, SDFT (stable and unstable version) and MSDFT methods in terms of the number of mathematical operations needed to update a single DFT bin (M is the number of samples within a window of length T).

Method name	Computational workload		Numerical stability
	Additions	Multiplications	
Short Time Fourier Transform (STFT)	M	M	✓
Sliding DFT (SDFT)	4	4	✗
Guaranteed-stable SDFT (rSDFT)	5	4	✓
Modulated Sliding DFT (MSDFT)	10	7	✓

DFT spectrum is used to estimate the synchrophasor (see for instance [51]), the so-called *Short-time Fourier Transform* (STFT) turns out to be very effective [3]. In both cases, the measurement reporting latencies are proportional to the amount of samples to be processed. As a consequence, the algorithm throughput can only be improved at the cost of deteriorating the PMU accuracy levels. The first option is to reduce the sampling rate and eventually originate aliasing; the other one refers to the adoption of shorter window lengths and potentially increase the spectral leakage effects [54].
In order to increase the throughput without decreasing the precision of the adopted DFT-based synchrophasor estimation algorithm, DFT can be calculated via recursive algorithms that are usually characterized by a lower number of operations to update the values of a single DFT bin (e.g., [4]). Despite this evident advantage with respect to the class of non-recursive DFT algorithms, the two categories do not generally have identical performances. In particular, the majority of the recursive algorithms suffers of errors due to either the approximations made to perform the recursive update, or the accumulation of the quantization errors produced by the finite word-length of computers [81].
A very effective method for sample-by-sample DFT bins computation, is represented by the so-called Sliding-DFT (SDFT) technique presented in [78]. This reference demonstrates the efficiency of this method in comparison with the popular Goertzel algorithm and its computational advantages over the more traditional DFT and FFT, but also its drawbacks. Unfortunately, the approach proposed in [78] is only marginally stable. If the truncation errors on the computation of the filter coefficients are not severe, the SDFT is bounded-input, bounded-output stable. Otherwise, the algorithm suffers from accumulated errors and is, consequently, potentially unstable. Whereas common approaches found in literature [78, 82] face this problem compromising results accuracy for guaranteed stability, the method proposed in [6] and called Modulated Sliding DFT (MSDFT) is guaranteed stable without sacrificing accuracy.
In what follows, three of the most efficient techniques to compute a portion of the DFT spectrum, namely the STFT, SDFT and MSDFT will be presented and analyzed with respect to their precision and computational complexity (see also Table 3.1).

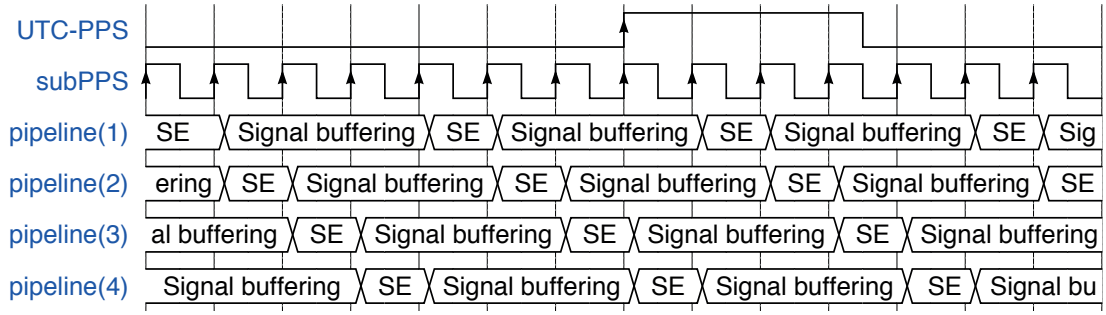


Figure 3.9 – Digital timing diagram of a hypothetical PMU that estimates synchrophasors 50 times per second using the STFT technique. A 4-stages pipeline is here adopted to achieve the desired reporting rate with a 3-cycles window to calculate the DFT and estimate the synchrophasor (SE stands for Synchrophasor estimation).

3.3.1 Short-time Fourier Transform

Starting from what formulated in equation (3.4), the DFT can be potentially updated every time-step n, based on the most recent set of samples $\{x(n-M+1), x(n-M+2), \ldots, x(n)\}$, according to the following time dependent equation:

$$X_k(n) = \sum_{m=0}^{M-1} x(q+m) \cdot W_M^{-km} \tag{3.30}$$

being M the number of samples within the window of length T[4], n the time-step index, k the DFT-bin index, $q = n - M + 1$ and $W_M^{-km} = e^{-j2\pi km/M}$ the DFT complex twiddle factor.
The derived equation is the so-called Short-Time Fourier Transform (STFT), namely the simplest technique to apply the DFT theory to a real signal. It assumes to split the signal into partially overlapping block of samples of equal length M and apply the DFT theory independently to each one of them. Consequently, such a calculation is extremely inefficient: although two consecutive estimations are derived from a partially overlapping windows, in order to update the DFT estimation, it assumes to re-process already analyzed portion of the signal.
Nevertheless, such a technique can still be applied to synchrophasor estimation, as long as the adopted hardware platform has enough available computational resources to host a parallel computation of the DFT according to equation (3.30) over the whole set of input channels and the PMU does not need to report estimated data too frequently. For instance, in order to achieve the highest IEEE Std. [1] reporting rates (i.e. a new estimation every nominal power system period) with a 3-cycles DFT-based synchrophasor estimation algorithm, one solution would be to apply the STFT calculation expressed by equation (3.30) to partially overlapped portions of data. These requirements can be satisfied by adopting a 4 stages pipeline architecture for each input channel. As shown in Fig. 3.9, based on the rising edges

[4] Henceforth in the thesis, and particularly when discussing about sliding window DFT calculation algorithms, N and M will be interchangeably used to make reference to the number of samples within a window of length T.

of a square waveform aligned to PPS and characterized by a frequency corresponding to the PMU reporting rate F_r, each pipeline will alternately collects the required amount of data (M samples) in dedicated memories and, once they have been filled, activates a flag that triggers the synchrophasor estimation on the previously acquired set of data.
Nevertheless, such an approach is characterized by evident limitations that are mainly related to the computational complexity and the high reporting latencies. In what follows two different approaches based on a sliding window and a sample-by-sample update of the DFT spectrum will be presented and commented in details.

3.3.2 Sliding DFT

The Sliding DFT structure is depicted in Figure 3.10a and, as demonstrated in [78], it can be derived from (3.4) as follows:

$$X_k(n) = \sum_{m=0}^{M-1} x(q+m) \cdot W_M^{-km} \tag{3.31}$$

$$= \sum_{m=0}^{M-1} x(q+m-1) \cdot W_M^{-k(m-1)} - x(q-1) \cdot W_M^{k} + x(q+M-1) \cdot W_M^{-k(M-1)} \tag{3.32}$$

$$= W_M^k \cdot \sum_{m=0}^{M-1} x(q+m-1) \cdot W_M^{-km} - x(q-1) \cdot W_M^{k} + x(q+M-1) \cdot W_M^{-k(M-1)} \tag{3.33}$$

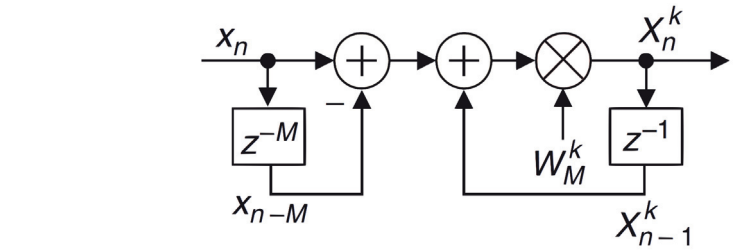
$$= W_M^k \cdot \big(X_k(n-1) - x(q-1) + x(q+M-1)\big) \tag{3.34}$$

$$= W_M^k \cdot (X_k(n-1) - x(n-M) + x(n)) \tag{3.35}$$

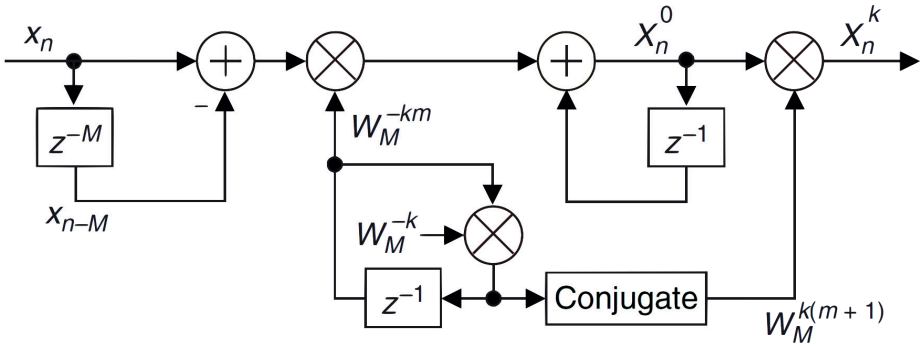
As it can be noticed by looking at equation (3.35), the SDFT is a quite efficient method as, it allows to update the values of a single DFT bin every time a new sample is acquired with few multiplication and additions (see Table 3.1 for the detailed analysis of the computational complexity of the SDFT method).
Unfortunately the SDFT filter is only marginally stable because its pole resides on the z-domain's unit circle [78]. In case the numerical rounding error related to the complex twiddle factor numerical representation is not severe, the SDFT is bounded-input, bounded-output stable. Otherwise, the algorithm suffers from accumulated errors due to numerical rounding and is, consequently, potentially unstable (see Figure 3.11). Common approaches that can be found in literature [78, 82] face this problem compromising results accuracy for guaranteed stability. This is the case of the method presented in [78] where the stability is guaranteed by including in the DFT formula a damping factor r that force the SDFT pole to reside within the z-domain's unit circle (this method is here referenced as rSDFT):

$$X_k(n) = r W_M^k \cdot \big(X_k(n-1) - r^M x(n-M) + x(n)\big). \tag{3.36}$$

In this context, the next Section will present a sample-by-sample DFT update method, called Modulated Sliding DFT (mSDFT) that is guaranteed stable without sacrificing accuracy [6].



(a)



(b)

Figure 3.10 – The structure of the Sliding DFT (a) and of the Modulated Sliding DFT (b) (adapted from [6]).

3.3.3 Modulated Sliding DFT

With reference to equation (3.35), it is easy to observe that the recursive formula for the computation of X_k when $k = 0$ does not involve the complex twiddle factor and is, therefore, by definition stable:

$$X_0(n) = X_0(n-1) - x(n-m) + x(n) \tag{3.37}$$

The mSDFT takes advantage of this SDFT-property in order to derive a recursive formula for the DFT computation that is intrinsically stable.
In particular, by taking advantage of the so-called Fourier modulation property (see Section A.3), the generic k-th DFT-bin can be shifted to the position $k = 0$ multiplying the input signal by the complex twiddle factor W_M^{-km}:

$$X_k(n) \xrightarrow{W_M^{-km}} X_0(n) = X_0(n-1) - x(n-M) \cdot W_M^{-k(m-M)} + x(n) \cdot W_M^{-km} \tag{3.38}$$

$$= X_0(n-1) + W_M^{-km} \cdot (-x(n-M) + x(n)) \tag{3.39}$$

where equation (3.39) is obtained thanks to the periodicity of the modulating sequence W_M^{-km}.
The twiddle factor modulation only introduces a phase shift that is changing with index m: $\angle W_M^{-km} = 0$ for $m = 0$, it increases by the W_M^{-k} factor at each iteration and is periodically reset

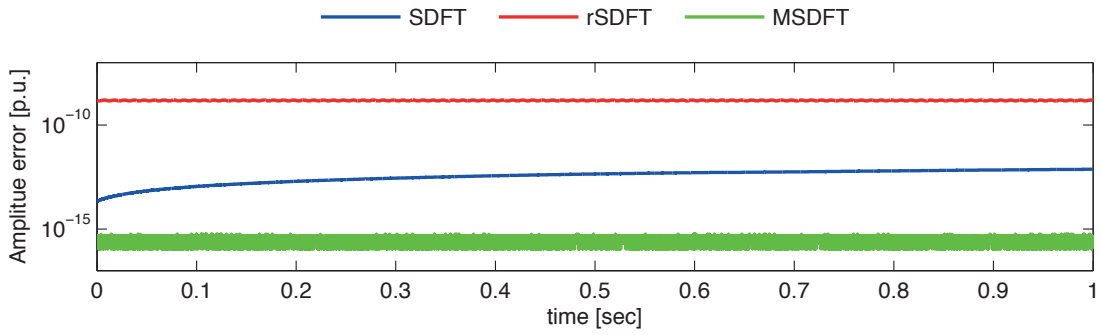


Figure 3.11 – The comparison between 3 sample-by-sample DFT update method: the Sliding DFT (SDFT, in blue), the guaranteed stable Sliding DFT (rSDFT, in red) and the Modulated Sliding DFT (MSDFT, in green). The SDFT numerical instability and the higher MSDFT precision with respect to the rSDFT method are evident.

to 0 every M samples. Indeed at every iteration the modulating sequence can be recursively computed as:

$$W_M^{-km} = W_M^{-k(m-1)} \cdot W_M^{-k}, \qquad m = 0, 1, \ldots, M-1 \tag{3.40}$$

It is clear that, in order to prevent that accumulated errors corrupt our estimation, the modulating sequence must be reset to 1 every M samples[5].
In view of this, the k-th bin of the DFT can be derived from equation (3.39), as:

$$X_k(n) = W_M^{k(m+1)} \cdot X_0(n) \tag{3.41}$$

$$= W_M^{k(m+1)} \cdot \left(X_0(n-1) + W_M^{-km} \cdot (-x(n-M) + x(n)) \right) \tag{3.42}$$

where $W_M^{-k(m+1)}$ compensate for the phase-shift due to the modulating sequence.
Equation (3.42) defines the MSDFT method for the update of the value of a single bin of the entire DFT spectrum and the related block scheme is given in Figure 3.10b.
To sum up, the comparison between the MSDFT and the other sample-by-sample algorithms presented in this Section is shown in Figure 3.11 in terms of their stability and accuracy.

Integrating the MSDFT with Signal Windowing

As already discussed in Section 3.2.4, signal windowing is a powerful technique that allows to reduce the effects of long-range spectral leakage. Windowing is applied as in the time-domain by weighting a finite sequence of samples with a particular window profile like the Hanning one (see Section 3.2.4):

$$x_w(n) = x(n) \cdot w(n), \quad 0 \le n \le N-1 \tag{3.43}$$

[5] To be noticed that, for practical implementation, the modulating sequence can be either (i) precomputed and stored into memory or (ii) computed online based on equation (3.40).

However, windowing by time-domain multiplication would compromise the computational simplicity of the MSDFT or any other sample-by-sample DFT calculation technique. For this reason, when adopting this kind of methods, it is of common use to apply the signal windowing in the frequency domain, namely after the DFT has been computed. Indeed, by recalling that the multiplication between two functions in the time-domain corresponds to the convolution between the Fourier transform of the two functions in the frequency domain (see equation (3.19)), the time-domain multiplication could be replaced by a frequency-domain convolution and obtain equivalent results.
In particular, in the case of the Hanning window, this will result into the following linear combination of adjacent DFT bins $X_k(n)$:

$$X_k(n) = -0.25 \cdot X_{k-1}(n) + 0.5 \cdot X_k(n) - 0.25 \cdot X_{k+1}(n) \tag{3.44}$$

From Equation (3.44), it is clear that, in order to compute 3 windowed DFT bins, we need to compute 5 MSDFT bins, namely those associated to indices $k_m + \{-2,-1,0,1,2\}$.

3.4 The Interpolated-DFT Technique

As demonstrated in the previous Section, DFT-based synchrophasor estimation algorithms are notoriously characterized by three main sources of uncertainty: aliasing, spectral leakage and spectral sampling.
Aliasing is usually corrected by two possible approaches: using adequate anti-aliasing filters or increasing the sampling frequency to values much larger than the highest spectrum component contained in the sampled signal.
On the other hand, spectral leakage arises when the sampling process is not synchronized with the fundamental tone of the signal under analysis and the DFT is computed over a non-integer number of cycles of the input signal [57]. Since accurately synchronizing the sampling process with the fundamental frequency component of the signal is purely theoretical, several approaches have been proposed to reduce this bias.
Among them the Interpolated-DFT (IpDFT) technique has outperformed the others for its higher accuracies combined with a lower computational complexity. Such a method refers to the usage of:

- windowing functions aiming at mitigating the effect of long-range spectral leakage [56];
- proper DFT interpolation schemes aiming at correcting the effects of the short-range leakage and reducing the inaccuracies introduced by the DFT spectral sampling (e.g., [51, 50]).

The IpDFT problem has been originally defined for a discrete sequence of samples windowed using the rectangular window [50]. In order to reduce the effects of long-range spectral leakage, the input sequence can be windowed using one of the “special” windowing functions defined

in literature. The first to combine such an approach with the IpDFT technique was Grandke in [51] using the Hanning window. More recently the IpDFT problem has been formulated using various windowing functions belonging to the Rife-Vincent class I (RVCI) [83] or parametric windowing function non belonging to the cosine windows class, like Kaiser Bessel or Doplh-Chebyshev windows [84].
In what follows the IpDFT algorithm will be first formulated and solved for the case of Hanning window; then its performances are analyzed, with a specific focus on the effect of the spectral interference on the accuracy of the IpDFT method.

3.4.1 Formulation of the IpDFT Problem

The Interpolated-DFT (IpDFT) is a technique that allows to estimate the parameters of a tone (i.e., its frequency, amplitude and phase) by interpolating the DFT spectrum obtained from a finite sequence of N samples of a discrete signal $x(n)$ that includes the tone under analysis.
In this respect, let's consider the following finite sequence obtained by sampling with a sampling rate $F_s = 1/T_s$ a continuous waveform $x(t)$ characterized by a single frequency component at frequency f_0:

$$x(n) = A\cos\left(2\pi f_0 n T_s + \varphi\right), \quad 0 \leq n \leq N-1. \tag{3.45}$$

The sequence $x(n)$ is then windowed with a specific windowing function $w(n)$ and its DFT computed following what stated in Section 3.2 and particularly equation (3.4).
As demonstrated in Section 3.2.3, if the window does not contain an integer number of periods of the signal $x(n)$ leakage occurs and the main tone of the signal will be located between two consecutive DFT bins (see Figure 3.12). Its frequency can therefore be expressed as follows:

$$f_0 = (k_m + \delta)\Delta f \tag{3.46}$$

being k_m the index of the the DFT bin characterized by the highest amplitude and $-0.5 \leq \delta < 0.5$ a fractional correction term.
From equation (3.46), the IpDFT problem can be formulated as follows:

> *Based on the DFT spectrum $X(k)$ of the signal $x(n)$ analyzed with the known windowing function $w(n)$, find the correction term δ that better approximates the exact location of the main spectrum tone.*

According to the adopted window profile and number of DFT bins used to perform the interpolation, various analytical or approximated solutions to the problem can be given [83]. In what follows the solution will be presented for a signal windowed using a Hanning window (see equations (3.25)-(3.27)) and using a 2-points interpolation.

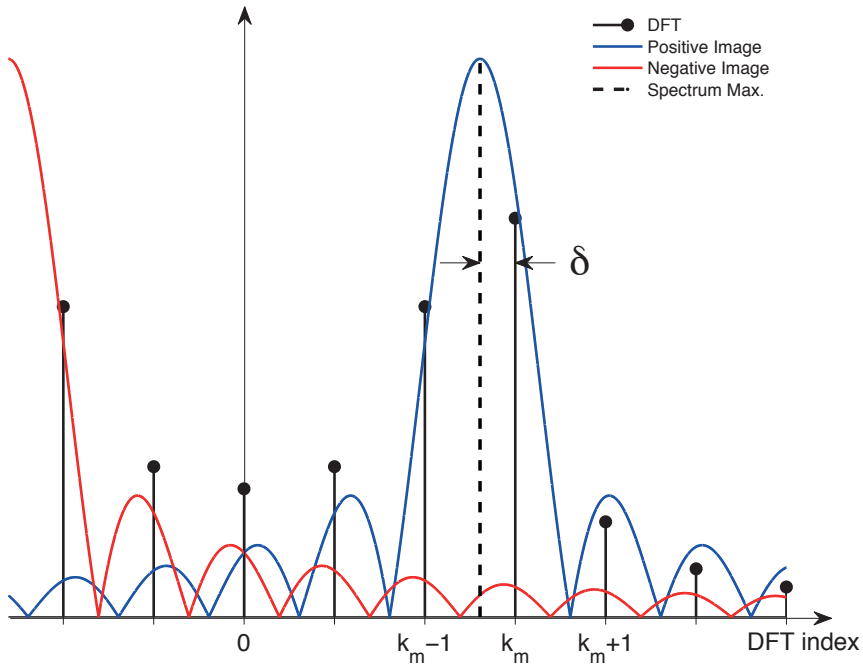


Figure 3.12 – Zoom on the portion of the DFT spectrum surrounding the highest bins that highlights the correction term δ and the spectral contributions produced by the positive (in blue) and negative image (in red) of the spectrum.

3.4.2 Solution of the IpDFT Problem using the Hanning Window

As demonstrated in Section 3.2, the spectrum of the sampled signal $x(n)$ in equation (3.45) can be expressed in terms of its positive and negative image:

$$X(f) = X^{+}(f) + X^{-}(f) \tag{3.47}$$

$$= \frac{A}{2} e^{j\psi} W_H(f - f_0) + \frac{A}{2} e^{-j\psi} W_H(f + f_0) \tag{3.48}$$

being $W_H(f)$ the Fourier transform of the Hanning window, A and ψ the amplitude and instantaneous phase of the signal $x(t)$ respectively.
Assuming that the effects of leakage are properly compensated by windowing, we can neglect the long-range spectral leakage produced by the negative spectrum image on the positive frequency range and assume that the DFT bins in the positive frequency range are only generated from the positive image:

$$X(k) \approx X^{+}(k), \quad 0 \leq k \leq \frac{N}{2} - 1. \tag{3.49}$$

The fractional term δ can be estimated starting from the ratio between the 2 highest bins of the DFT $X(k_m)$ and $X(k_m + \varepsilon)$ that, for $N \gg 0$ can be approximated as follows (see [83] for

further details):

$$\frac{X(k_m+\varepsilon)}{X(k_m)} \approx \frac{W_H((\varepsilon-\delta)\cdot 2\pi/N)}{W_H(-\delta\cdot 2\pi/N)} \tag{3.50}$$

where $W_H(\cdot)$ is the Fourier transform of the Hanning window (see equation (3.26)) and

$$\varepsilon = \begin{cases} 1 & \text{if} |X(k_m+1)| > |X(k_m-1)|, \\ -1 & \text{if} |X(k_m+1)| < |X(k_m-1)|. \end{cases} \tag{3.51}$$

According to what demonstrated in Appendix A.2, the modulus of $W_H(\cdot)$ can be approximated as:

$$\begin{aligned} |W_H(\omega)| \approx & |\sin(\omega N/2)| \cdot \\ & \cdot \left| -\frac{0.25}{\sin(\omega/2-\pi/N)} + \frac{0.5}{\sin(\omega/2)} - \frac{0.25}{\sin(\omega/2+\pi/N)} \right| \end{aligned} \tag{3.52}$$

By replacing (3.52) in (3.50) and recalling that $\lim_{x\to 0}\sin(x) = x$ we get:

$$\begin{aligned} \frac{X(k_m+\varepsilon)}{X(k_m)} &= \frac{|W_H((\varepsilon-\delta)\cdot 2\pi/N)|}{|W_H(-\delta\cdot 2\pi/N)|} \\ &\approx \left| \frac{0.25}{\delta-\varepsilon+1} - \frac{0.5}{\delta-\varepsilon} + \frac{0.25}{\delta-\varepsilon-1} \right| \Big/ \left| \frac{0.25}{\delta+1} - \frac{0.5}{\delta} + \frac{0.25}{\delta-1} \right| \\ &= \dots \\ &= \left| \frac{0.5}{\delta(\delta-\varepsilon)(\delta-2\varepsilon)} \right| \left| \frac{\delta(\delta+1)(\delta-1)}{-0.5} \right| \\ &= \left| \frac{\delta+\varepsilon}{\delta-2\varepsilon} \right| \end{aligned} \tag{3.53}$$

that, solved for the frequency correction δ gives:

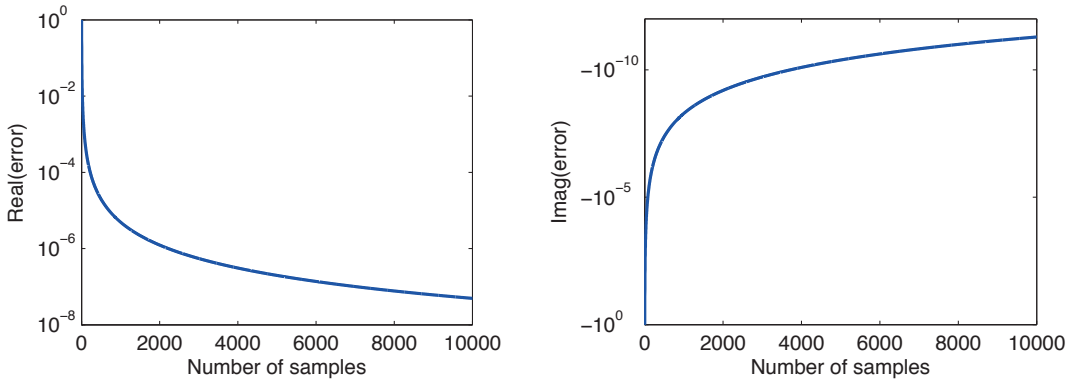
$$\widehat{\delta} = \varepsilon \, \frac{2|X(k_m+\varepsilon)| - |X(k_m)|}{|X(k_m)| + |X(k_m+\varepsilon)|} \tag{3.54}$$

where the $\widehat{\ }$ symbol was used to stress the fact that this is an estimation of the fractional correction term δ. The waveforms parameters (i.e., its frequency, amplitude and phase) can then be computed as follows:

$$\widehat{f} = (k_m + \widehat{\delta})\Delta f \tag{3.55}$$

$$\widehat{A} = |X(k_m)| \left| \frac{\pi\widehat{\delta}}{\sin(\pi\widehat{\delta})} \right| \left| \widehat{\delta}^2 - 1 \right| \tag{3.56}$$

$$\widehat{\varphi} = \angle X(k_m) - \pi\widehat{\delta} \tag{3.57}$$



(a) (b)

Figure 3.13 – Behavior of the real(a) and imaginary part (b) of $e^{\pm j\pi(N-1/N)} - (-1 \pm j\pi/N)$ (see equation (3.58)) as a function of the number of samples N.

3.4.3 The IpDFT Uncertainty Sources

Even if the IpDFT is a powerful method to artificially increase the DFT frequency resolution, its accuracy is prone to various sources of error that need to be properly discussed. Indeed the sources of uncertainty that affect the performances of such a method can already be identified based on the assumptions (i.e., approximations) that has been made to solve the related problem. These assumptions involve properties of the original signal $x(t)$ and the relevant DFT spectrum $X(k)$ that do not always hold in the real world and might introduce several levels of uncertainty to an ideal unbiased estimation of the IpDFT method.
In what follows the sensitivity of the IpDFT method to the above-mentioned approximations is analyzed and properly commented.

IpDFT Sensitivity to the Number of Samples N

As demonstrated in Appendix A.2, the IpDFT solution given in equation (3.54) for the case of the Hanning window can only be obtained if the number of samples N is sufficiently large so that the following approximation is valid:

$$e^{\pm j\pi(N-1/N)} \approx -1 \pm j\pi/N \tag{3.58}$$

Figure 3.13 shows the residuals of equation 3.58. As it can be seen, by adopting a relatively high sampling rate F_s the number of samples N can be increased up to values where the effects of such an approximation are not visible and it can be considered exact.

IpDFT Sensitivity to Transient Events

The signal $x(t)$ must be stationary within the adopted window length, i.e. its parameters must be constant, in order to correctly interpret the DFT spectrum. If a transient occurs, the DFT hypothesis do not hold any longer and the DFT spectrum cannot be correctly interpreted to estimate the tone parameters via IpDFT.
The only solution to guarantee such an hypothesis is to adopt a window length that is sufficiently short so that the signal can be assumed stationary within it.

IpDFT Sensitivity to Spectral Interference

The spectral interference is a major source of uncertainty for any IpDFT technique, as it generally does not allow to distinguish the portion of spectrum that has been generated by the tone under analysis from other frequency components. Eventually, if the energy content of the spectral interference exceed the one of the tone under analysis, the tone detectability is not even guaranteed.
For this reason, any IpDFT technique, usually assumes that both the spectral interference generated by nearby tones (harmonics and inter- or sub-harmonics) and the one produced by the relevant negative image(s) on the positive frequency range are negligible, so that the portion of DFT spectrum under analysis could be assumed to be generated from the positive image of the tone under analysis only.
In order to reduce as much as possible the effects of spectral interference, the use of windows with good side-lobes behavior (see, for instance, [85]) is usually suggested. Nevertheless, when the IpDFT technique is applied to the analysis of tones that are concentrated in the lower range of DFT frequencies, the above mentioned approach might not guarantee acceptable accuracies. This is due to the proximity of the positive and negative images in the frequency spectrum and therefore to the relatively high spectral interference that the negative image generates on the positive one.
In this respect, the following of this Chapter will focus on the formulation of a synchrophasor estimation algorithm that enhances the IpDFT performances by combining such a technique with an iterative approach for the compensation of the spectral interference produced by the negative image of the main tone of the spectrum.

3.5 The Iterative IpDFT Technique for Synchrophasor Estimation

Synchrophasor estimation algorithms that are based on the IpDFT technique typically adopt relatively high sampling rates with respect to the tone under analysis, usually in the order of some tens of kHz. This choice is justified by the fact that, particularly in Distribution Networks, the higher harmonic distortion might cause major interference if aliasing is not properly taken into account by a sufficiently high sampling rate. Additionally, in the case of IpDFT algorithms that adopt the Hanning window, higher sampling rates allow to process a number of samples $N \gg 0$ and correctly approximate the complex exponential in equation

(3.58), also when shorter window length are adopted. The latter, in the case of SE based on the IpDFT technique, rarely exceed 5 periods of a signal at the nominal frequency f_0. This is because longer windows might "mask" the power system dynamic event and increase the PMU response times way above the acceptable limits. Moreover, longer time windows might not comply with the response time limits dictated by [1], particularly with respect to the P-class measurement requirements.
Therefore the DFT spectrum that is calculated from a finite sequence of samples of a voltage/current waveform obtained with these values of sampling rate and window length, concentrates its energy in the lower range of frequencies. Consequently, the positive and negative images of the spectrum are relatively close each other (see Figure 3.12) and the spectral interference produced by the negative image of the spectrum on the positive frequency range represents a major source of uncertainty when estimating the synchrophasor. This is due to the fact that the main approximation that was made to derive the formula for the calculation of δ (namely that the spectral interference produced by the negative image can be neglected, see equation (3.49)), no longer holds and the bins $X(k_m)$ and $X(k_m+\varepsilon)$ are not only originated by the positive image of $x(t)$ but also influenced by the tails produced by the negative image of the spectrum [50]. This phenomenon can be slightly reduced by adopting windowing functions with good side-lobe behaviors [85] that, unfortunately, are not sufficient to achieve higher accuracies that are needed in Distribution networks (see Chapter 2).
The performances of any IpDFT method are definitely related to the accuracy in the estimation of the fractional term δ that, ideally, could be improved by processing a DFT spectrum that only contains the positive image of the tone under analysis. In this respect, in what follows, an iterative technique for the compensation of the spectral interference produced by the negative image of the main tone of the spectrum is proposed and combined with the IpDFT technique based on the Hanning window (see Section 3.4.2) to derive a novel SE algorithm that hereafter will be called iterative-Interpolated DFT (i-IpDFT).

3.5.1 Iterative Compensation of the Spectral Interference

By neglecting the spectral interference produced by other tones, the DFT spectrum of the signal $x(n)$ in equation (3.45) can be expressed, as shown in equation (3.47), in function of the contribution of the positive and negative images of the main tone. As a consequence, the highest and second-highest DFT bins, which are used to estimate δ according to equation (3.54), can be expressed as:

$$X(k_m) = \frac{1}{B}\left[\frac{A}{2}e^{j\psi}\cdot W(-\delta) + \frac{A}{2}e^{-j\psi}\cdot W(2k_m+\delta)\right], \tag{3.59}$$

$$X(k_m+\varepsilon) = \frac{1}{B}\left[\frac{A}{2}e^{j\psi}\cdot W(\varepsilon-\delta) + \frac{A}{2}e^{-j\psi}\cdot W(2k_m+\varepsilon+\delta)\right] \tag{3.60}$$

where $W(\cdot)$ is the Fourier transform of the adopted windowing function and the spectral interference coming from the negative spectrum image is represented by the following terms:

$$X^{-}(k_m) \triangleq \frac{1}{B}\left[\frac{A}{2}e^{-j\psi}\cdot W(2k_m+\delta)\right], \tag{3.61}$$

$$X^{-}(k_m+\varepsilon) \triangleq \frac{1}{B}\left[\frac{A}{2}e^{-j\psi}\cdot W(2k_m+\varepsilon+\delta)\right] \tag{3.62}$$

Since $W(\cdot)$ is analytically known once the windowing function has been selected, the amount of spectral interference generated by the negative image of the spectrum on the above DFT bins can be estimated. In particular, equations (3.61) and (3.62) can be evaluated using an initial estimation of the waveform parameters $\widehat{A}$ and $\widehat{\psi}$ obtained using the classical IpDFT technique presented in Section 3.4.2. This amount can then be subtracted from the DFT bins to reduce the spectral interference so that the "compensated" DFT bins

$$\widehat{X}(k_m) = X(k_m) - X^{-}(k_m) \tag{3.63}$$

$$\widehat{X}(k_m+\varepsilon) = X(k_m+\varepsilon) - X^{-}(k_m+\varepsilon) \tag{3.64}$$

are mostly generated by the positive image of the spectrum.
Then, the estimation of the fractional term δ and the related waveform parameters can be improved and used, eventually, to improve the estimation of the spectral interference produced by the negative spectrum image. This process can be either iterated a predefined number of times or performed until a given convergence criterion is achieved and bring to a more accurate and final estimation for the set of parameters $\{\widehat{f},\widehat{A},\widehat{\psi}\}$.

3.5.2 Formulation of the i-IpDFT Method

The proposed SE algorithm combines a classical IpDFT technique based on a Hanning window with the method described in the previous section for the iterative compensation of the spectral interference produced by the negative image of the spectrum. The pseudo-code reported in the next page explains the fundamental steps necessary to correctly estimate the synchrophasor according to the i-IpDFT technique.
First, the continuous input waveform (voltage or current) is sampled with a sampling rate F_s that is sufficiently high to neglect the effects of aliasing on the DFT spectrum (see Section 3.2.3). For sake of clarity, in the following of the thesis we will make reference to a sampling rate F_s = 50 kHz. The samples are then collected into a finite sequence of length N that should be sufficiently short so that the signal can be assumed stationary at least within its boundaries. In this respect a window containing three periods of a signal at the nominal frequency f_0 (namely $T = NT_s = 3/f_0$) has proven to be a good trade-off between the accuracy and response-time requirements [86]. The finite sequence of samples is then windowed using a Hanning window and the three highest bins of the DFT, namely those corresponding to DFT

Algorithm 2 The iterative IpDFT synchrophasor estimation algorithm.

procedure ITERATIVE INTERPOLATED DFT($x(t)$) ▷ $x(t)$ is the input signal
  Signal sampling: $x(n) = x(nT_s)$ ▷ Sampling rate: $F_s = 1/T_s = 50$ kHz
  Signal buffering: $x(n), \quad n = 0, \ldots, N-1$ ▷ Window length $T = NT_s = 3/f_0$
  Signal windowing (Hanning): $x_h(n) = x(n) \cdot w_H(n)$ ▷ see equation (3.25);
  DFT calculation: $X(k), \quad k = k_m + \{-1, 0, +1\}$ ▷ see equation (3.4);
  2-points DFT Interpolation: $\{\widehat{f}, \widehat{A}, \widehat{\psi}\}_0$ ▷ see equations (3.55)-(3.57);
  for $r = 1 \rightarrow R$ **do**
    Spectral interference estimation: $X^-(k_m)$, $X^-(k_m + \varepsilon)$ ▷ see eq. (3.61), (3.62) ;
    DFT enhancement: $\widehat{X}(k_m)$, $\widehat{X}(k_m + \varepsilon)$ ▷ see equations (3.63),(3.64);
    2-points DFT Interpolation: $\{\widehat{f}, \widehat{A}, \widehat{\psi}\}_r$ ▷ see equations (3.55)-(3.57);
    if $\{\widehat{f}, \widehat{A}, \widehat{\psi}\}_r \approx \{\widehat{f}, \widehat{A}, \widehat{\psi}\}_{r-1}$ **then**
      break **for**
    end if
  end for
  return $\{\widehat{f}, \widehat{A}, \widehat{\psi}\}_r$
end procedure

indexes $k = k_m + \{-1, 0, +1\}$, computed according to what stated in equation (3.4)[6].
Next, a first estimation of the parameters of the main tone can be given according to the classical 2-points IpDFT technique based on a Hanning window formulated in Section 3.4.2. Although such an estimation could be considerably affected by the effect of the spectral interference produced by the image component, it can be used to approximate the effects of its "tails" on the two highest DFT bins that are used to estimate δ according to what stated in the previous Section 3.5.1. Such an amount can be subtracted from the original DFT spectrum to reduce the effect of spectral interference and the waveform parameters estimation refined. As shown in the pseudo-code, this approach is either iterated a predefined amount of time or until the spectral interference compensation does not bring any additional advantage.
As it can be noticed, the i-IpDFT technique has a clear advantage with respect to other SE methods: the algorithm is composed by few well-defined macro-functionalities that are often recalled along the execution of the pseudo-code through a for loop structure. As it will be demonstrated in the next Chapter, the i-IpDFT SE algorithm can therefore exploit the speed of Field programmable Gate Arrays (FPGAs) and reduce the required amount of hardware resources simply reusing already allocated portion of the hardware design.

3.5.3 Effects of the Number of Iterations on the i-IpDFT Estimations

In this Section the effects of the number of iterations on the estimated synchrophasor accuracy will be demonstrated in both static and dynamic conditions. In particular, the results make reference to two test conditions defined in the IEEE Std. C37.118, namely the *signal frequency*

[6] It is worth pointing out that by adopting a sufficiently short window length T, the index corresponding to the DFT maximum k_m can be fixed a priori and calculated as $k_m = \lceil f_0/\Delta f \rfloor = \lceil f_0 N/F_s \rfloor$. Consequently there is no need to perform a maximum search on the DFT bins.

test (see Section 1.3.4) and the *System Frequency Ramp* test (see Section 1.3.5). The reference signals have been synthesized in a software environment where the previously presented i-IpDFT technique has been also implemented. These tests were chosen because they are those in the IEEE Std. [1] that magnify the effects of spectral interference and therefore the tests where the i-IpDFT method should mostly improve the performances of classical IpDFT methods.
The performance of the synchrophasor estimation are shown in function of the frequency, amplitude and phase estimation errors as stated in Section 1.3.3. In particular, in order to combine multiple plots in a single graph, the simulation results have been presented in a logarithmic scale and therefore the above errors are presented in terms of their absolute value.

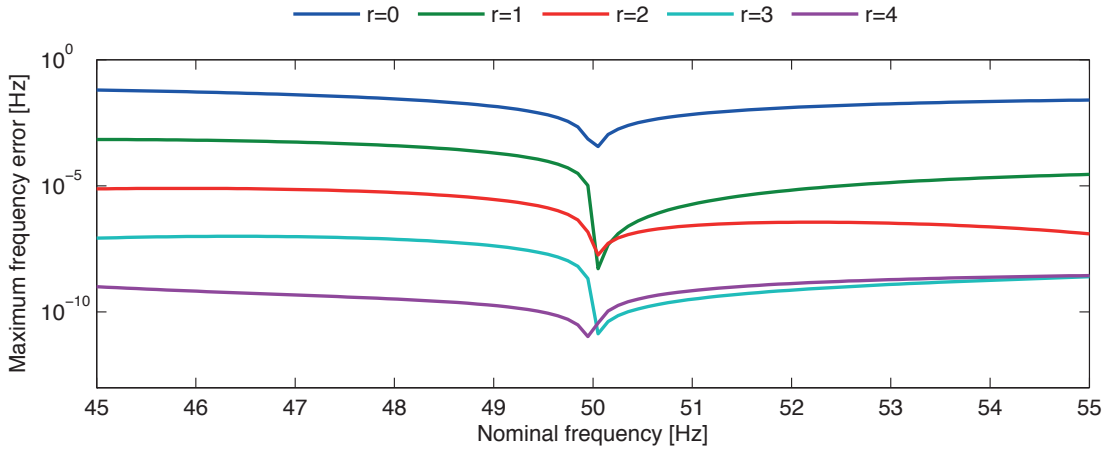
Steady-state performances

The improvement introduced by the i-IpDFT in steady-state conditions are presented during the signal frequency test (see Section 1.3.4) with a nominal frequency of 50 Hz; nevertheless equivalent results can be obtained for 60 Hz. The i-IpDFT performances are shown in function of the nominal frequency of each sub-test that, in the case of a 50 Hz power system, must span the frequency interval between 45 and 55 Hz.
In particular Figure 3.14 shows the maximum frequency, amplitude and phase errors for various number of iterations (i.e., the parameter r in Algorithm 2), starting from $r = 0$ (i.e., the classical IpDFT approach without any compensation of the spectral interference) up to $r = 4$. The effects of the iterative compensation of the spectral interference produced by the negative image of the spectrum are evident and self-explanatory: the estimation accuracies of frequency, amplitude and phase are improved of almost two orders of magnitude every new iteration, up to the 4^{th}. After, the effects of the spectral interference compensation are no longer visible.
Additionally, it is possible observing that, independently of the number of iterations, the best accuracies are obtained for $f \approx f_0$ (namely for values of frequency closer to 50 Hz) since the effects of spectral leakage interference are here minimized. They deteriorate as the nominal frequency of each sub-test deviates from the rated one f_0 and the effects of spectral interference increase. In particular, the i-IpDFT accuracies are asymmetric with respect to f_0; in other words the frequency interval on the left of f_0 usually exhibit poorer performances than the frequency interval on the right of f_0. The cause of this behavior is still related to the spectral interference produced by the negative image spectrum that is higher as the two images get closer, namely for smaller nominal frequencies. Nevertheless, such an asymmetry between the frequency intervals on the left and on the right of f_0 is relative and becomes less and less visible by increasing the number of iterations.
Finally Figure 3.15 compares the performances of the i-IpDFT synchrophasor estimation algorithm with those provided by the classical IpDFT technique that adopt the Hanning window during the signal frequency test. In particular the 5 (blue-dashed line), 4 (green-dashed line), 3 (red-dashed line) and 2-periods (light blue-dashed line) IpDFT SE techniques are compared to the 3 (red-continuous line) and 2-periods (light-blue continuous line) i-IpDFT

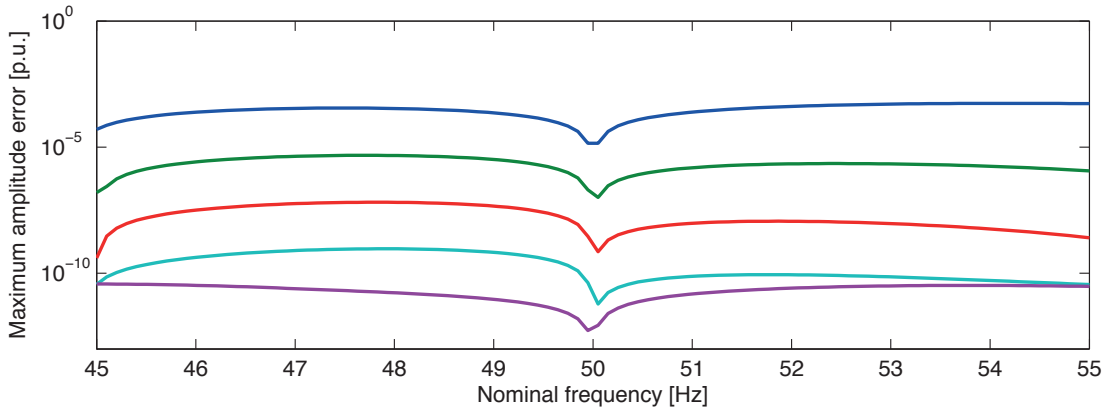
SE techniques that adopt 4 and 7 iterations respectively.
As it can be noticed the classical IpDFT accuracy are strongly related to the adopted window length and, due to the higher immunity to spectral leakage, the longer the window length the higher the steady state accuracies. On the other hand, the i-IpDFT technique definitely improves such an accuracy and, at the same time, allows to reduce the window length down to 2-periods of a signal at the nominal frequency f_0. Such a possibility, introduces non-negligible advantages as it allows to considerably reduce the PMU response times and measurement reporting latencies (see Section 1.3.3) without deteriorating the PMU accuracies.

Dynamic performances

The improvement introduced by the i-IpDFT technique during dynamic conditions can be evaluated by making reference to the frequency ramp test, defined in the IEEE Std. C37.118 (see Section 1.3.5). During this test the frequency of the reference signal is linearly increased from 45 to 55 Hz at a rate of 1 Hz/s.
Figure 3.16 shows the instantaneous errors in the estimation of frequency amplitude and phase during a positive frequency ramp (the results for the negative ramp are here omitted but leads to equivalent conclusions) for various number of iterations. Similarly to the previous figure, the blue line is obtained for $r = 0$ and makes reference to a classical IpDFT technique where the effects of the spectral interference are neglected. The other two lines are the result of the i-IpDFT with one and two iterations respectively. Also during this test the improvements introduced by the iterative compensation of the spectral interference produced by the negative image of the tone are evident and lead to enhanced accuracies of the estimated synchrophasor that can reach accuracies similar to those obtained during steady-state. In particular, the effects of the iterative compensation presented in Section 3.5.1 are visible up to the third iteration in the case of the estimated value of frequency and amplitude and up to the second iteration for the estimated phase.



(a)



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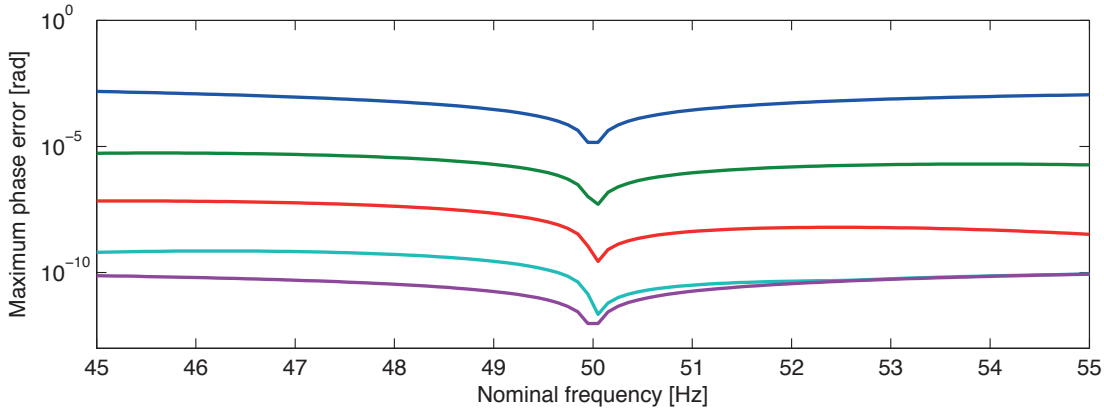
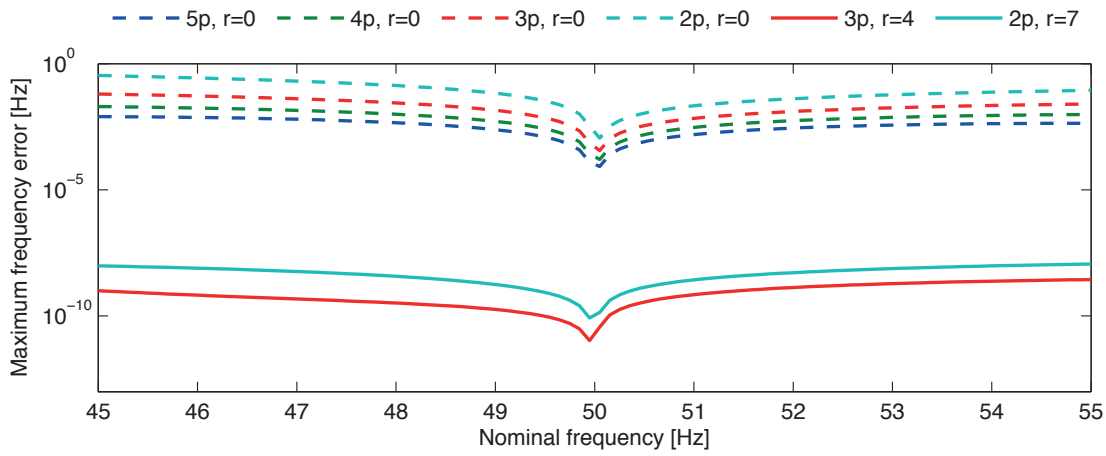
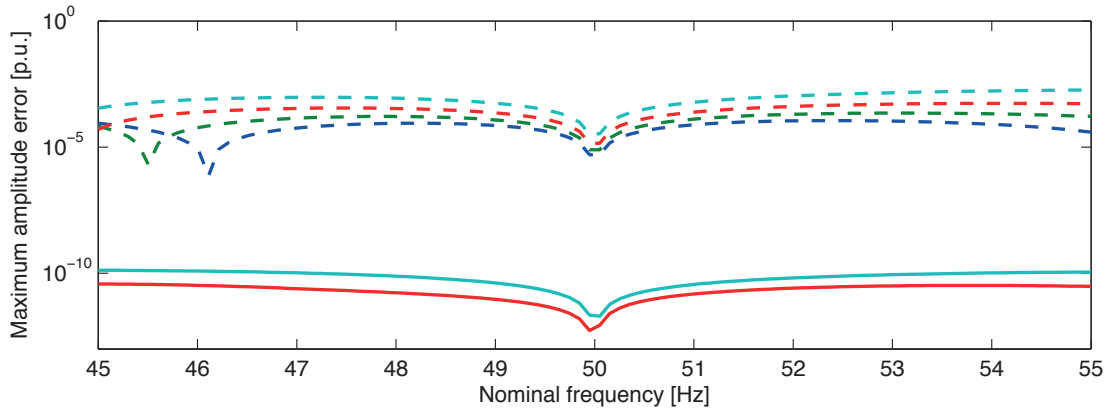


(c)

Figure 3.14 – The maximum frequency (a), amplitude (b) and phase estimation errors (c) of the proposed i-IpDFT method as a function of the nominal frequency of a steady-state reference signal. The errors are plotted for various number of iterations ($r = 0, 1, 2, 3, 4$), being $r = 0$ the classical IpDFT method.



(a)



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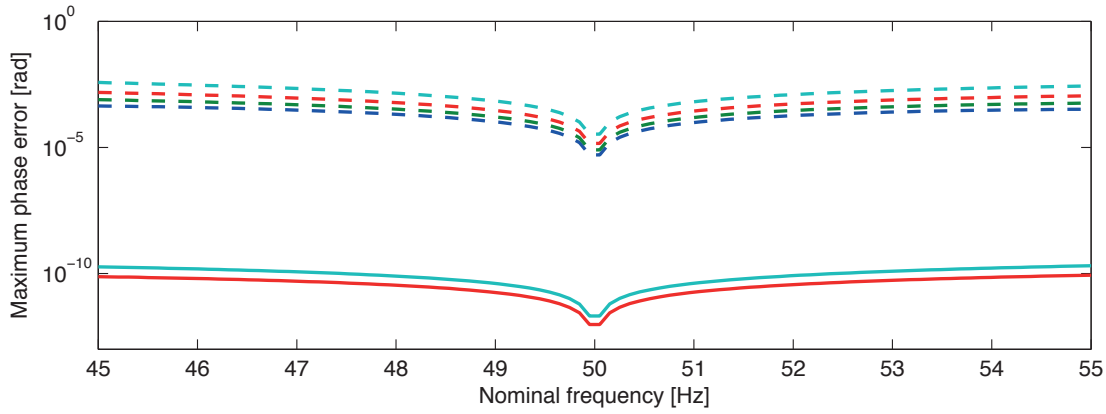
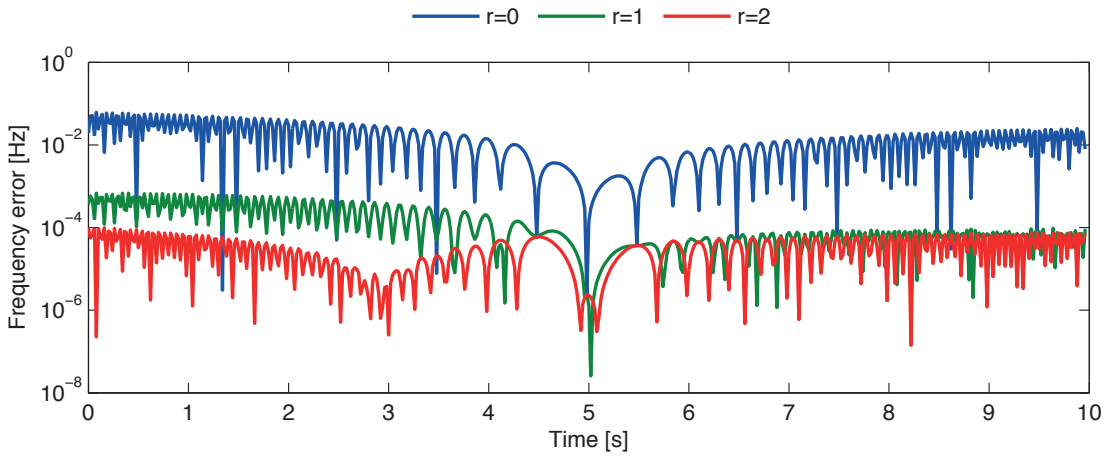
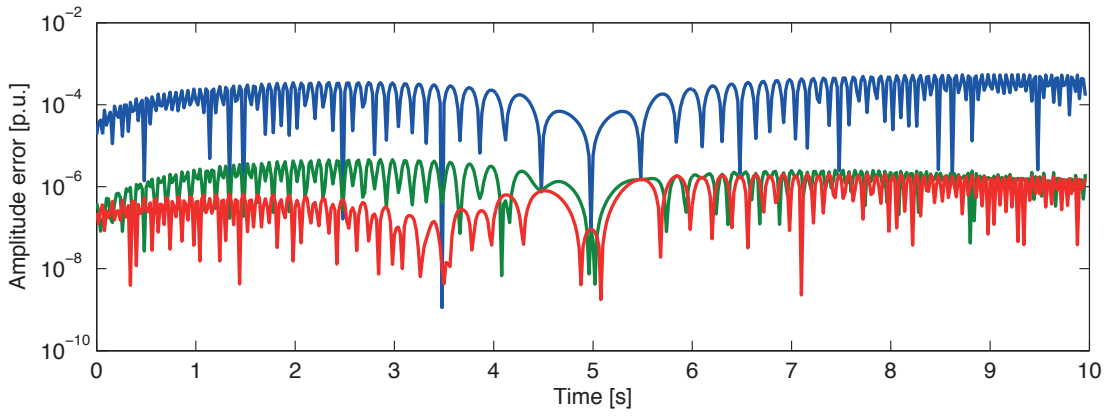


(c)

Figure 3.15 – The maximum frequency (a), amplitude (b) and phase estimation errors (c) of the proposed i-IpDFT technique versus the classical IpDFT approach, as a function of the nominal frequency of a steady-state reference signal. The graphs present the results for 5- (blue), 4- (green), 3- (red) and 2-periods (light blue) IpDFT estimators with (continuous) and without (dashed) the proposed iterative compensation of the spectral interference.



(a)



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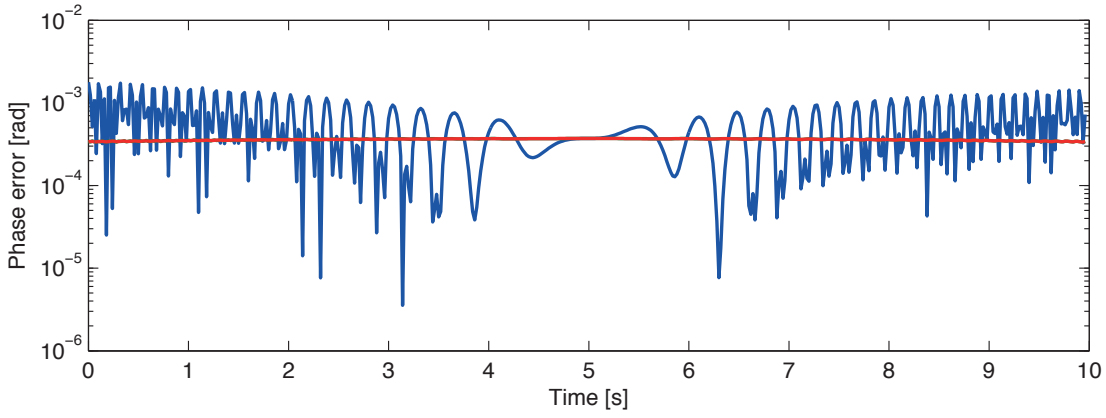


(c)

Figure 3.16 – The instantaneous frequency (a), amplitude (b) and phase estimation errors (c) of the proposed i-IpDFT technique during a positive frequency ramp of the system frequency. The errors are plotted for various number of iterations ($r = 1, 2, 0$), being $r = 0$ the classical IpDFT method.

4 Development of a PMU Prototype Based on the i-IpDFT Technique

This chapter discusses the development of a PMU prototype based on a Xilinx Zynq System-on-Chip (SoC), a hardware platform that combines the flexibility of a real-time processor with the high-speed and intrinsic determinism of a Field Programmable Gate Array (FPGA). The Chapter illustrates the non-trivial aspects related to the deployment of the proposed i-IpDFT synchrophasor estimation algorithm into such an embedded platform, with a particular focus on the synchronization of the developed PMU prototype to the UTC-time reference provided by the GPS.

4.1 Hardware and Software Requirements Specification

The design of any system must start from the requirements specification. With respect to the PMU prototype to be developed, three main criteria have been defined: *accuracy, speed* and *costs*.

The *accuracy* requirements have already been discussed in the context of this thesis. The proposed PMU prototype must first of all satisfy most, if not every IEEE Std. C37.118 requirement in both static and dynamic conditions (see Section 1.3), as the IEEE Std. compliancy is a first step towards the adoption of such a technology in DNs. Furthermore, the PMU must be characterized by increased steady-state and transient accuracies to allow its deployment in ADNs, whose characteristics have been extensively described in Chapter 2. As a consequence, the developed i-IpDFT SE algorithm must be carefully integrated in the whole PMU framework, combining sufficiently accurate A/D converters and a time-sync unit that is capable of keeping stable and precise synchronization in most operating conditions.

Costs are another crucial parameter that will determine if PMUs will be adopted by DNOs to monitor their power distribution system. Indeed, the the amount of nodes (i.e., substations) that can be potentially equipped with PMUs is much higher in DN rather than Transmission networks. Nevertheless, DNOs typically manage a lower capital compared to the investment that typical TNOs are used to put in place. As a consequence a PMU designed to be installed in

DNs must satisfy an additional requirement, namely the cost. This should be definitely lower than the usual planned investments for substation automation that, usually, never exceed the 10 k$ per substation.
Last but not least the *speed* is another important requirement as the proposed PMU must be capable of reporting synchrophasor at rates that eventually could exceed those defined in [1] and with reduced measurement reporting latencies. This would allow to use the PMU data streams not only for offline post-processing applications, but also for real-time applications that require more stringent reporting latencies, above all, power system protections.
Indeed, such an application might take major advantages from the availability of PMU data. In this respect, the literature already contains several contributions related to real-time fault identification and location processes using synchrophasors[74, 75, 87, 88]. The majority of these methods assumes a centralized approach where PMUs stream data to a Phasor Data Concentrator (PDC), that processes them in order to identify and locate the fault with the minimum possible latency. If the centralized approach is adopted, in order to keep, at least, the same latencies characterizing existing relay-based protection schemes, the involved PMU technology has to satisfy additional requirements compared to those introduced by the IEEE Std. C37.118.1-2011 [1] and its latest amendment C37.118.1a-2014 [8]. In particular, it needs to estimate and report real-time synchrophasor-data with sufficient time-determinism, lower time-latencies and higher refresh rates without sacrificing their accuracy that has, at least, to keep the same levels dictated by [1] and [8]. Since the time spent in estimating the synchrophasor usually represents one of the main burden within the whole PMU-based measurement chain, it is definitely necessary to develop faster synchrophasor estimation algorithms.

4.2 The Adopted Hardware Platform

As described in Section 1.1.4, a generic PMU must include the following hardware components:

- *A/D converters* that sample the voltage/current waveforms at a sampling rate F_s;
- a *time-sync unit* that receives and decodes a UTC-time reference signal disseminated using any of the techniques presented in Section 1.2.2;
- one or more *processing units* that host at least the following two functionalities: (i) a real-time implementation of a specific synchrophasor estimation technique; (ii) the data encapsulation and streaming process;
- at least, one *network adapter* that allows to stream the estimated data to a Phasor Data Concentrator.

These components should be carefully selected to allow a feasible deployment of the basic PMU functionalities presented in Section 1.1.4 and particularly in Figure 1.3, and not to degrade further the performances of the adopted SE algorithm. In what follows, the selected

PMU hardware components will be presented and combined together to build-up the final hardware platform that will be used to develop the PMU prototype.

4.2.1 Processing Unit and Enclosure

Even though, as discussed in Section 1.1.4, each one of the PMU hardware components contributes to the global uncertainty of the PMU estimations, the processing unit represents the core of a PMU. This is because such a component is dedicated to combine the various information coming from the other elements into a sufficiently accurate synchrophasor estimation that will be then streamed to external applications.
The processing unit mainly implements the synchrophasor estimation algorithm ,namely a Digital Signal Processing (DSP) technique that allows to extract the synchrophasor from a set of samples of the input waveforms. Traditionally, digital signal processing algorithms were most commonly implemented using general-purpose (programmable) DSP chips (e.g., General Purpose Processors – GPP) for low rate applications, or special-purpose (fixed function) chip-sets for higher rates applications. The latter include, in order of ease of programmability (namely the ability to use the same hardware to implement different DSP algorithms): Digital Signal Processors (DSP), Graphical Processing Unit (GPU) and Application-Specific Integrated Circuit (ASIC).
Nevertheless, the latest technological advancements in Field Programmable Gate Arrays (FPGAs) during the past 10 years have opened new paths for DSP design engineers. Indeed FPGAs maintain the advantages of the high specificity of the ASIC while avoiding the high development costs and inability to make design modifications after production. At the same time FPGAs increase the performances of standard DSP processors due to their higher clock speed and intrinsic parallelism. Additionally, further to the more recent integration of DSP blocks, like embedded Multiply and Accumulate (MAC) logic, into the FPGA chip-set, this technology has become a common platform to deploy DSP algorithms.
Nevertheless FPGAs lack of the inner flexibility characterizing GPPs. For these reasons, quite recently, FPGAs have been integrated with real-time processors in single chip-sets called System on Chip (SoC). Such a configuration combines the increased performances, hardware determinism and reliability of FPGAs with the flexibility of general purpose processors that run a real-time operating system (RTOS) to handle lower-frequency control loops or provide internet connectivity and facilitate remote data access, system management, and diagnostics.
In this respect, the developed PMU prototype is based on the Xilinx Zynq 7020 SoC that combines:

- a 667 MHz dual-core ARM Cortex-A9 processor characterized by 1 GB of nonvolatile data storage and 512 MB DDR3 memory;
- an Artix 7 FPGA characterized by 106400 flip-flops, 53200 6-inputs look-up-tables (LUT), 560 kilobytes of embedded RAM and 220 programmable DSP blocks (i.e, 18x25 bits MAC);

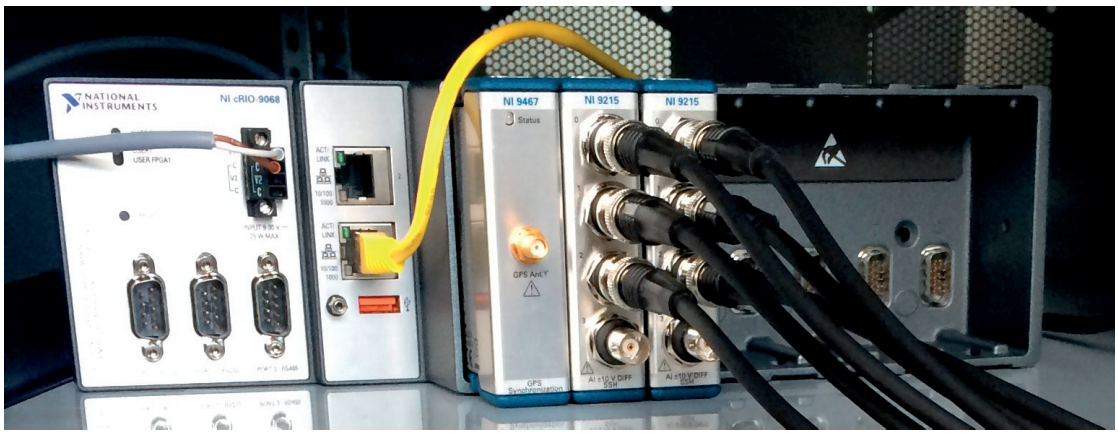


Figure 4.1 – The PMU prototype based on the NI-9068 compactRIO platform equipped with the Xilinx Zynq 7020 SoC and the following input modules: one NI-9467 GPS receiver and two NI-9215 Successive Approximation Register (SAR) low -voltage (±10 V) ADC modules.

- two 10/100/1000 Mbps Ethernet adapters.

To facilitate the development of the PMU, it has been chosen to enclose such a chip-set in the National instrument compactRIO Chassis NI-9068 [89] that is equipped with a dedicated distribution of a Linux Real-Time OS and allows the possibility to connect up to 8 input modules that can be customized to the user's needs (see Figure 4.1).

4.2.2 GPS receiver

The developed PMU prototype has been equipped with a stationary GPS receiver to provide the necessary synchronization to a UTC time-reference. Indeed, as discussed in Section 1.2, this is the most commonly adopted absolute time-reference for PMUs due to its good compromise between performances and costs and to the relatively high availability and coverage. In this respect, the choice has felt on the compactRIO module NI-9467 [90], a stationary GPS receiver characterized by a datasheet accuracy of ±100 ns, a standard value for terrestrial GPS receivers. The GPS unit has been metrologically characterized in the Time and Frequency Laboratory of the University of Neuchatel, Switzerland. To this end, the unit has been integrated into the compactRIO chassis NI-9068 and configured to generate, through an NI-9402 digital output module, a GPS-synchronized 500 kHz square waveform. This signal has been compared to a 10 MHz time reference generated by an EFOS-13 Hydrogen MASER by means of a 3120A Phase noise test probe by Symmetricom [91], a frequency and phase analyzer that allows to measure the Allan deviation of any periodic signal connected to its inputs (see Section 1.2.1). In this respect Figure 4.2 shows, in a log-log scale, four different measurements of the Allan Deviation of the selected GPS receiver, namely:

- in blue, a 400 seconds Allan deviation measurement taken just after the first GPS-signal "locking" event (in this condition the GPS receiver has not yet reached its nominal

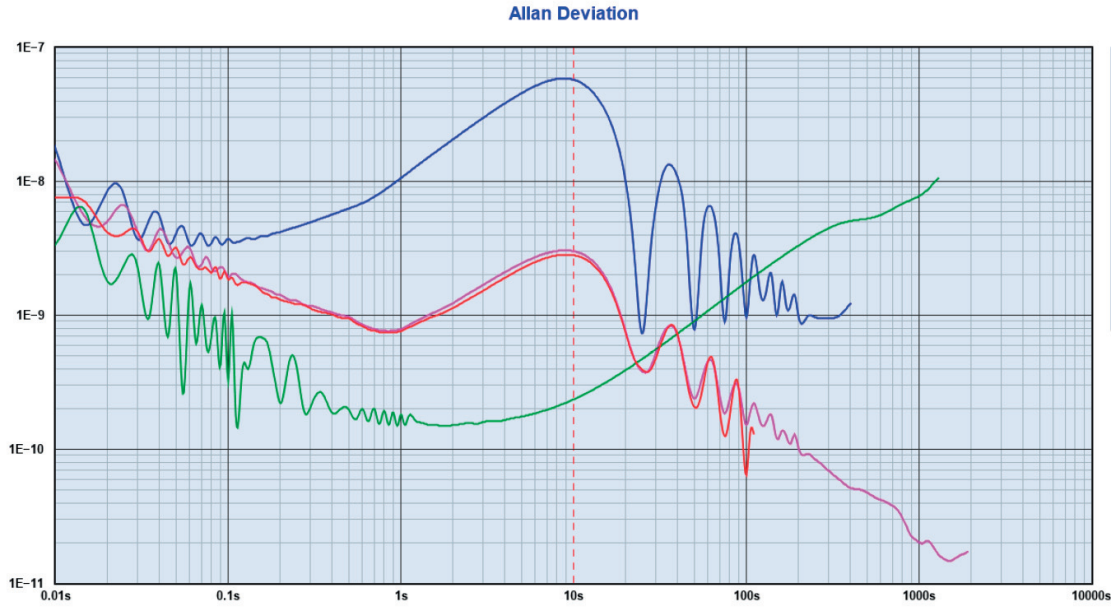


Figure 4.2 – Four different measurements of the Allan deviation of a GPS-synchronized 500 kHz square waveform generated through the GPS receiver NI-9467. In blue a 400 seconds measurement taken just after the first GPS-locking event; in red and pink two different measurements of 100 and 2000 seconds respectively taken after 10 minutes the first GPS-locking event; in green a 1400 seconds measurement when the module is disconnected from the GPS antenna.

accuracy due to the internal logic of the controller);

- in red and pink two measurements of 100 and 2000 seconds respectively, of the Allan deviation taken about 10 minutes after the GPS "locking" event (i.e., the GPS receiver is assumed to have reached a steady-state);
- in green a 1400 seconds Allan deviation measurement obtained when the GPS module is disconnected from the GPS antenna and the signal generation is let "free-running".

The following behaviors can be highlighted by observing the various Allan deviation measurements:

- The frequency variations during the first 400 seconds after the GPS "locking" event (i.e., blue curve) are remarkable (i.e., up to $5 \cdot 10^{-8}$[s/s]), particularly in the range between 0.1 and 10 s. As a consequence the PMU estimations during this preliminary phase must be tagged with specific time-quality flags (see [18]) that identify the poor quality of the transmitted data.
- By looking at the "cusp" of both red and pink curves, it is evident that the GPS receiver operates with a time-constant of 10 s. Afterwards, both measured Allan deviations are characterized by a standard $1/\tau$ slope.

- Every curve exhibits various oscillations that can been ascribed to the GPS module firmware. In particular, this software libraries implement a PID (proportional-integral-derivative) controller that aligns the internal oscillator to the GPS time reference and generates such an oscillatory behavior.

- By comparing the green, pink and red curves, it is evident that when let free running, the GPS receiver generates a frequency-drifting signal that is nevertheless characterized by a better short-term stability (i.e., in the range between 0 and 20 s). In other words the GPS receiver and its software libraries deteriorates the short-term accuracy of the free running FPGA quartz oscillator.

In general, the selected GPS receiver represents a good solution for its good trade-off between performances and costs. Nevertheless, the PMU performances might be improved by adopting a GPS unit that embeds a more stable oscillator (e.g., a TCXO, see Section 1.2) and equipped with a firmware that does not deteriorate its performances.

4.2.3 A/D converters

The PMU has been configured to accept two different set of A/D converters based on the instrument transformer technology used to interface the PMU to the high voltage/current signals of the power system to which it is connected.
The first configuration adopts the 16-bits Successive Approximation Register (SAR) ADC technology that is embedded in the NI-9215 compactRIO module [92]. This 4-channels low-voltage (±10 V) input module can sample the input signal with sampling rates up to 100 kS/s and is characterized by higher accuracy and reduced latencies. Such a configuration is intended to be coupled with advanced voltage and current sensors developed for distribution network installations (see for instance [93]) that typically output low-voltage signals (1-10 V).
On the other hand, the second configuration adopts the 24-bits Delta-Sigma ADC technology that is embedded in both NI-9225 [94] (voltage) and NI-9227 [95] (current) compactRIO module. These modules are used to sample high voltage (300 V_{RMS}) and current (5 A_{RMS}) signals respectively with sampling rates up to 50 kS/s. They are equipped with built-in anti-aliasing filters with a pass-band of $0.453 \cdot F_s$ and a stop-band starting at $0.547 \cdot F_s$. This configuration is intended to be used in combination with standard instrument transformers (voltage and current) that typically output signals at nominal 100 V and 1 A.
Whereas the developed PMU prototype supports both module configurations, the digital design and experimental validation presented in Chapter 4, make reference to a PMU equipped with the second set of modules (i.e., the NI-9225 and NI-9227 for voltage and current signals respectively).

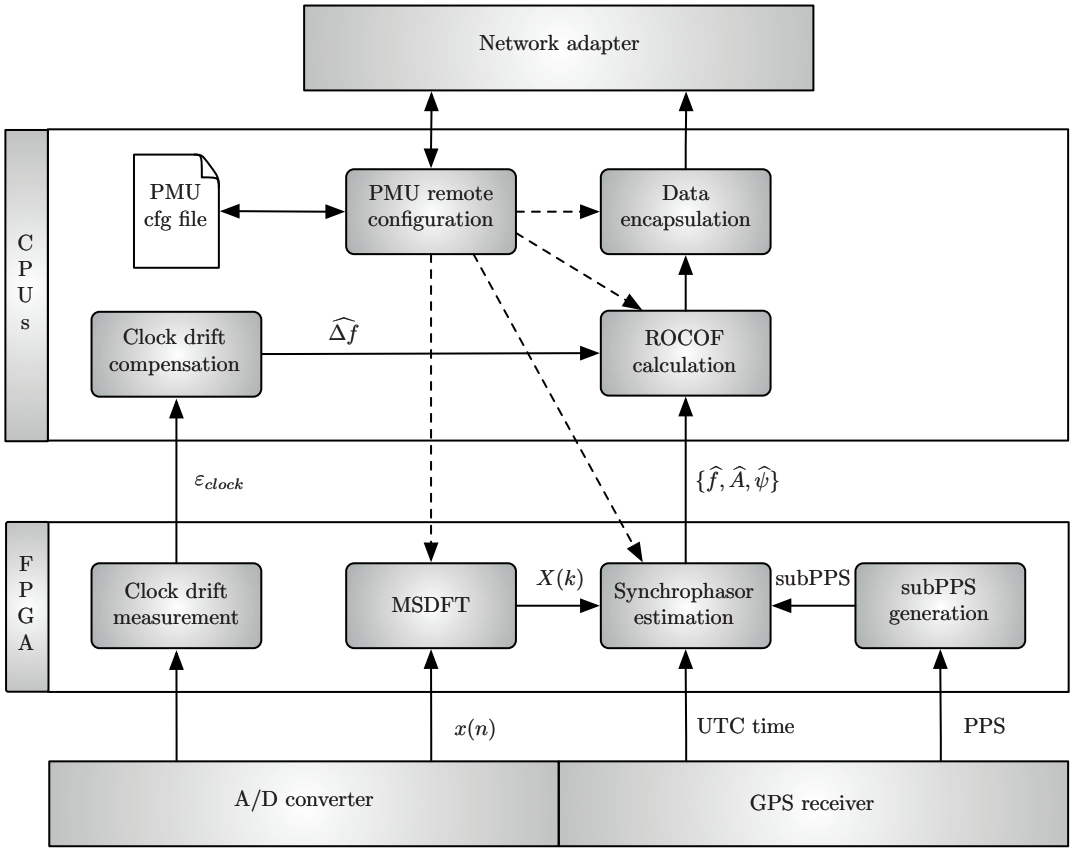


Figure 4.3 – The PMU design in terms of the software modules deployed in the FPGA and in the ARM processor and their inter-dependencies.

4.2.4 System Overview

The developed PMU appears as shown in figure 4.1 and is characterized by extremely reduced sizes (10 × 10 × 30 cm), another non-negligible advantage when the PMU need to be installed in MV substations that might be quite "packed".
In this specific configuration the GPS and ADC modules are installed in the first 3 available slot respectively but, if needed, 5 more slots are available to process additional input channels. The input modules directly communicate with the FPGA through a dedicated backplane. The SE algorithm has been fully deployed on the FPGA to take advantage of the higher speed and determinism of the calculations. The estimated synchrophasors are then transferred to the dual-core ARM processor through dedicated Direct Memory Access (DMA) channels. Here the data are encapsulated according to the transmission protocol specified in the IEEE Std. C37.118.2-2011 and streamed out through one of the two available Ethernet adapters. The compactRIO chassis accepts on the left a standard DC power source (9-30 V, 25 W max) to power-up the system. Both the user led and the GPS module led can be used to visually check the status of the system.

The software modules for both FPGA and the RT processor have been designed according to Figure 4.3 and using the LabVIEW software environment for FPGA and RT targets respectively. In what follows each one of the developed software modules will be accurately presented and its performances analyzed.

4.3 FPGA Design and Resources Allocation

The FPGA digital design is a quite delicate process that needs to take into account both hardware limitations and application requirements. In Figure 4.3 the main software component that have been deployed in the FPGA portion of the PMU are depicted and the main interactions highlighted.
As already mentioned, the DSP logic, and particularly the i-IpDFT SE algorithm described in Section 3.5, has been completely integrated in the FPGA target and has been physically separated from the data streaming and PMU configuration logics that are hosted in the more suitable dual-core ARM processor. In particular, the FPGA controls both the ADCs and GPS receiver and continuously receives a stream of samples $x(n)$ from the various input channels. The samples from each input channel are then cut in sections and used to calculate a portion of the DFT in real-time. To this end, many techniques have been presented in Section 3.3 with respect to the real-time calculation of such numerical tool. Among them, the MSDFT has been selected, for its improved throughput compared to the traditional STFT and for its inherent numerical stability and accuracy compared to other sample-by-sample DFT calculation methods. The calculated DFT samples $X(k)$ are then transferred to a parallel process that, synchronously with a PPS-aligned trigger signal (hereafter called subPPS), estimates the waveform parameters according to the i-IpDFT technique. This information is combined with the UTC time-stamp received from the GPS receiver to obtain a stream of synchrophasors that are pushed, through dedicated DMA channels, to the real-time processing units.
In parallel a process monitors the status of the A/D conversion process and particularly, measures the eventual drift of the ADC sampling clock. This value is regularly (once per second) transmitted to the ARM processor that opportunely compensate the estimated synchrophasors.
The following Subsections will present and analyze each FPGA software module.

4.3.1 MSDFT Deployment

The use of FPGA to deploy and run a sample-by-sample DFT calculation technique like the MSDFT (see Section 3.3.3), is strongly suggested, due to the higher speed and determinism of such an hardware platform. Indeed the MSDFT is an extremely efficient sample-by-sample DFT calculation technique that assumes that for each new sample, every DFT bin is updated in order not to compromise the next DFT estimations. This computation must be performed before the acquisition of the next sample, over the whole set of PMU input channels, in order to correctly estimate the corresponding synchrophasors. Since the PMU technology has to

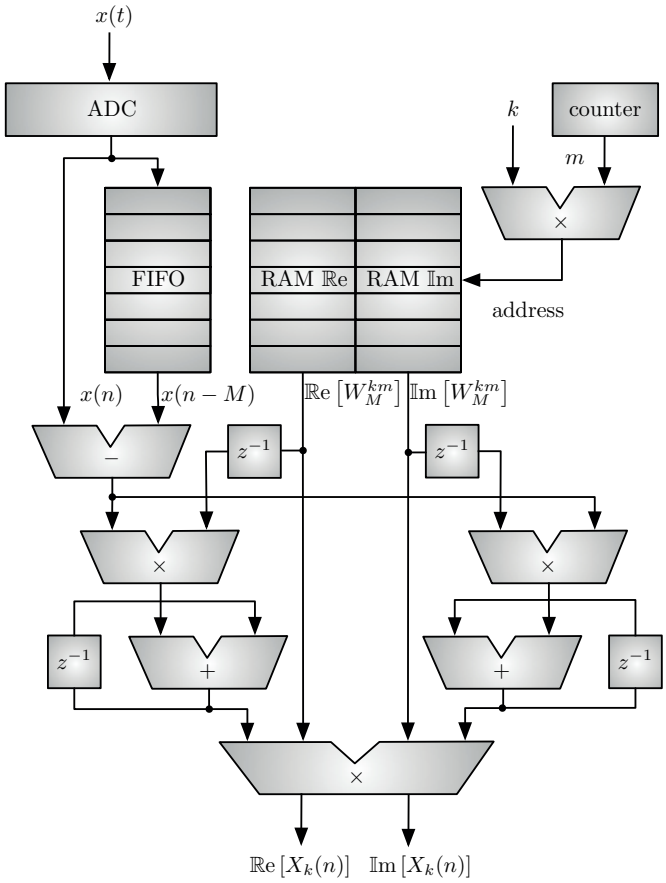


Figure 4.4 – FPGA Logical blocks needed to compute a single DFT bin by means of the MSDFT algorithm presented in Section 3.3.3. In particular the proposed design adopts blocks of RAM to store the MSDFT coefficients, a counter to access the memory locations and standard MAC and registers to compute the DFT.

provide estimations with a very high degree of confidence, the platform that will host the MSDFT algorithm need to guarantee a certain level of determinism.
Additionally, as demonstrated in Appendix A.4, the stability of the MSDFT is only guaranteed when implemented using a fixed-point representation. In this respect the use of FPGA to implement the i-IpDFT SE algorithm is not only further justified but also strongly recommended.
In what follows the deployment of the MSDFT algorithm in the FPGA-based PMU prototype defined in Section 4.2 is presented with particular focus on the FPGA resources allocation.
A minimum set of FPGA logical blocks needed to implement the MSDFT algorithm for the update of a single DFT bin is shown in Fig. 4.4 together with the relevant interconnections. The analog signal $x(t)$ is digitally converted by an A/D converter to provide the digital sequence of samples $x(n)$. As shown in equation (3.39), the MSDFT has to keep memory of the last M samples in order to compute the difference $x(n) - x(n-M)$. This can be done by means of a FIFO (First-In-First-Out) memory. In parallel, every time a new sample comes, a modular counter increments the value of the index $m \in [0, M-1]$. This, together with the value of the

Table 4.1 – FPGA compilation results for the MSDFT (1-bin and 5-bins calculation) and the i-IpDFT (results obtained setting $r = 1$). The results are expressed in terms of the used number of DSP blocks (one DSP block contains a 18×25 multiplier), blocks of RAM (one block of RAM can store up to 32 kbits of data), look-up-tables (LUTs) and flip-flops. The associated computation latency is also reported.

FPGA component	DSP	RAM	LUTs	Flip-Flops	Latency [µs]
MSDFT (1-bin)	41	7	17,090	16,200	0.5
MSDFT (5-bins)	41	7	19,041	17,966	2.5
i-IpDFT (SE only)	81	0	16,991	15,236	19.2
Total Available	220	140	53,200	106400	-

DFT bin to be computed, returns the address of the memory location of the a pre-allocated RAM that contains the instantaneous values of the twiddle factor W_M^{km}, expressed in terms of its real and imaginary part. Rather then recomputing the twiddle factor at every iteration, such a solution has two main advantages: (i) it saves execution time by sacrificing the occupation of the available blocks of RAM inside the FPGA; (ii) the twiddle factor computation does not suffer of any accumulated errors. Once the above listed operations completed, the k-th DFT bin $X_k(n)$ can be updated based on equations (3.39), and (3.42) separately for real and imaginary part.

Based on the block scheme of Figure 4.4, the MSDFT method for the estimation of a single DFT bin was deployed in the FPGA. As it can be noticed from the compilation results shown in the first row of Table 4.1, only with the allocated resources for the update of a single DFT bin via MSDFT, the number of used DSP blocks raises up to 41. Since we need to compute 5 bins of the DFT spectrum, by replicating 5 times the previously designed block we would get very close to the FPGA physical limits and would not be able to add on top of that the e-IpDFT algorithm. Hence the calculation of the 5 DFT bins needs to be serialized by sharing the portion of the FPGA dedicated to the MSDFT computation with every DFT bin and sacrificing the algorithm latencies for the FPGA area requirements. Since the latency of the proposed MSDFT implementation is very small (0.5 µs) this choice would not add much in term of measurement reporting latency.

The compilation results of a 1-channel MSDFT that computes 5 DFT bins, namely those associated to the DFT indices $k_{max} + \{-2, -1, 0, 1, 2\}$, based on the above explained logic, are shown in the second row of Table 4.1. As expected, the usage of FPGA logic blocks does not significantly change compared to the single DFT update, whereas the latency increases by exactly a factor of 5. To be noticed that the extension to more than 1 input channel will only increase the amount of used RAM needed to keep memory of the latest M samples for each input channel. On the other hand, the amount of memory needed to store the pre-computed twiddle factor will not change, as well as the amount of used DSP blocks.

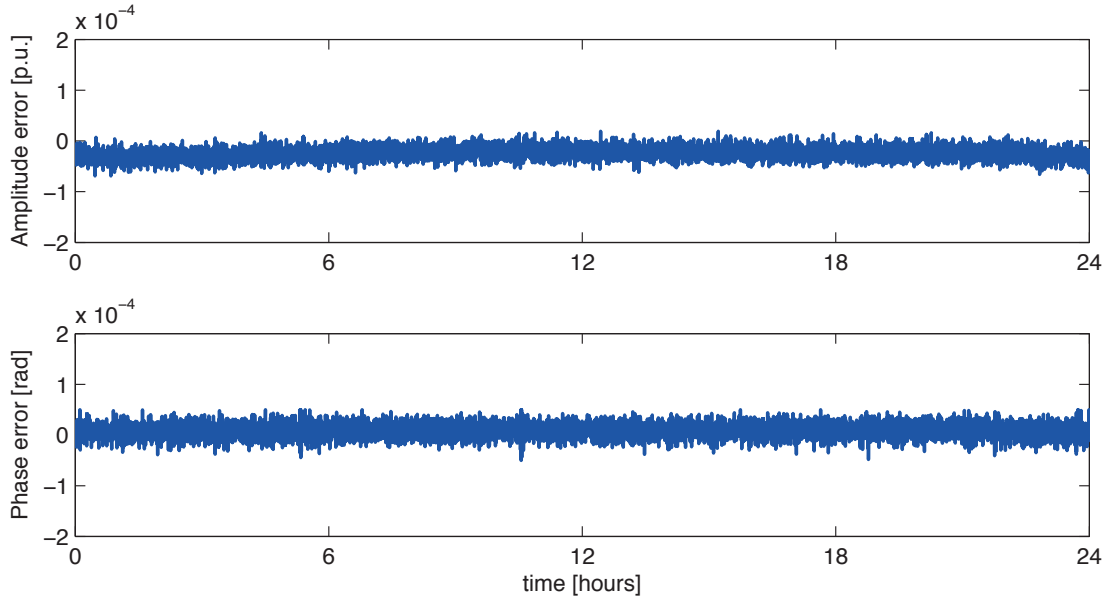


Figure 4.5 – Results of a 24 hours test aimed at verifying the numerical stability of the MSDFT when used to calculate the highest bin of the spectrum. As it can be noticed, the MSDFT amplitude and phase estimations do not drift over time, meaning that the FPGA design presented in Section 4.3.1 is numerically stable.

MSDFT Numerical Stability Verification

In order to verify the numerical stability of the proposed MSDFT implementation, a steady-state 50 Hz reference signal was synthesized by a GPS-synchronized National Instrument PXI system (see Chapter 5 for further details on the reference signal generation technique) and acquired by the compactRIO running the MSDFT as described in Section 4.3.1 for the calculation of the highest bin of the spectrum. Such a setup has been left running for 24 hours to exclude any numerical instability of the MSDFT. The estimated values of amplitude and phase were recorded on the compactRIO and compared with the reference phasors generated by the PXI system. Figure 4.5 shows the errors over the 24 hour test. As it can be noticed the estimations do not show any instability and the proposed MSDFT design can be considered correct.

4.3.2 i-IpDFT Deployment

The proposed i-IpDFT SE algorithm assumes that the original signal is windowed with a Hanning window, in order to reduce the effects of the long-range spectral leakage. Nevertheless, as discussed in Section 3.3.3, signal windowing cannot be directly applied in the time-domain when the MSDFT is used to calculate the DFT and must be moved in the frequency-domain. For this reason the MSDFT calculation and the i-IpDFT synchrophasor estimation algorithm can be decoupled and run in two separate processes. In this respect, whereas the MSDFT

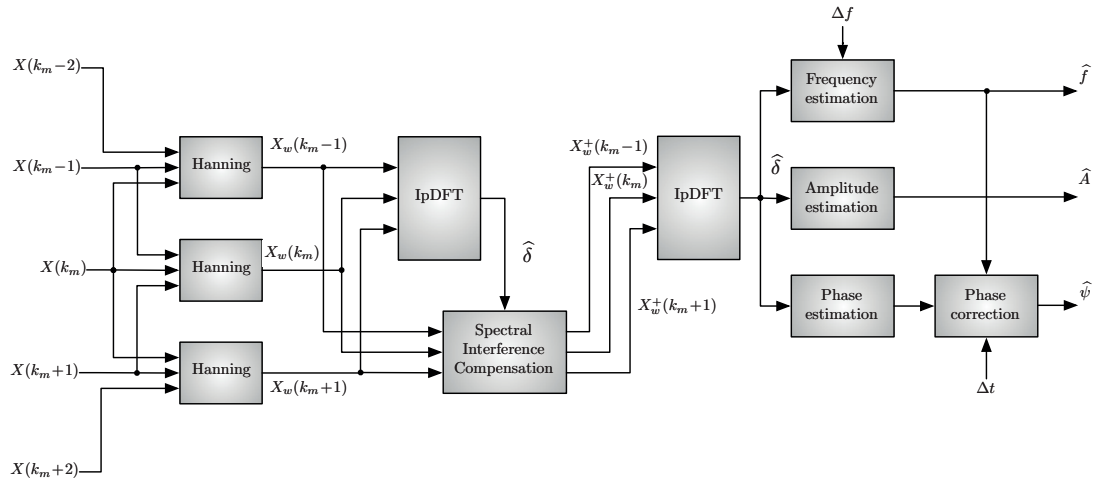


Figure 4.6 – Block scheme that shows how the i-IpDFT was deployed on the adopted FPGA-based PMU prototype. The scheme makes reference to a single iteration to compensate the effects of the spectral interference produced by the negative image of the spectrum (see Section 3.5.1).

process, as discussed in Section 3.3.3, must be executed every time a new sample is acquired, the i-IpDFT can run less frequently, according to the reporting rate settings of the PMU. The two processes communicate by means of a shared portion of the available RAM in the FPGA. The MSDFT process regularly updates the values of a portion of the DFT spectrum composed by the five bins that are needed to estimate the synchrophasor (see Section 3.3.3) and the i-IpDFT process reads them according to the rising edge of a periodic square waveform, hereafter called subPPS, characterized by a frequency corresponding to the PMU reporting rate (see Section 4.3.3 for further details about the subPPS waveform).

The i-IpDFT algorithm was deployed in the FPGA according to the block scheme shown in Figure 4.6 where each block corresponds to a well-identified functionality or group of equations. The five DFT bins are first processed according to equation (3.44) to obtain three Hanning-windowed DFT bins that are used to give a first estimation of $\widehat{\delta}$ according to a 2-points DFT interpolation expressed by equation (3.54). The estimated $\widehat{\delta}$ is then used, together with the known Hanning window profile $W_H(k)$ to estimate the spectral interference that is then subtracted from the DFT bins (see equations (3.61)-(3.64)). These can now be considered being generated from the positive image only and therefore the application of the IpDFT will produced improved estimates of the synchrophasors according to equations (3.55)-(3.57). As it can be noticed such an implementation uses a single iteration ($r = 1$) to compensate the effects of the spectral interference produced by the negative image of the spectrum.

The FPGA resources were allocated in order to reuse logic blocks that are recalled multiple times within the i-IpDFT algorithm. This is the case, for instance, of the Hanning windowing and the estimation of δ according to the IpDFT theory. The compilation results of the synchrophasor estimation process only are shown in Table 4.1 for a PMU equipped with a single

input channel. The characteristic latency of this portion of the FPGA is of only 19.2 µs. Such a low latency to estimate the synchrophasor value of a single input channel allows to estimate the synchrophasor of each input channel in series, namely one after each other. Even though the overall SE latency will rise to $C \cdot 19.2$ µs, being C the number of input channels (voltage and/or current) this approach will allow to keep the same amount of allocated FPGA resources independently of the processed number of channels.

4.3.3 UTC Synchronization of the PMU Estimations

As known, synchrophasor measurements need to be referenced to a common UTC-time source in order to provide accurately time-tagged measurements [1].
Regardless of the chosen UTC synchronization technology, several approaches to provide synchronized measurements of synchrophasor, frequency and ROCOF exist. In general, they can be separated in two categories:

- approaches where the sampling process is directly synchronized to UTC-time, for instance, by disciplining the ADC oscillator to the UTC time-reference provided by the GPS receiver;
- approaches that adopt a free-running sampling process and where the synchronization is performed "a-posteriori".

It is obvious that the first solution is generally more advisable: by directly associating a time-stamp value to each sample and by aligning the sampling process to the PPS, the synchronization is automatically achieved. In practice, if we assume that the latest acquired sample $x(n)$ is characterized by a UTC time-stamp value $t(n)$, based on the above-described procedure, the synchrophasor's time-stamp $t_s(n)$ is the time corresponding to the middle of the time window of length T containing the set of samples $\{x(n-M),\ldots,x(n-1)\}$. It can be computed as:

$$t_s(n) = t(n-1) + T_s - T/2 \tag{4.1}$$

where T_s is the PMU sampling time.
Nevertheless, depending on the selected platform, such an approach is not always feasible and therefore the second approach must be adopted. This is the case, for instance, of the selected compactRIO-based PMU platform when coupled with the NI-9225 Delta-Sigma converter (see Section 4.2.3). Indeed such an ADC is equipped with an internal oscillator that is not directly accessible from the compactRIO platform. As a consequence, it is mandatory to adopt the second technique where the ADC is left free running.
According to this technique, the synchronization of the PMU estimations to UTC-time can be performed by internally synthesizing a square waveform, hereafter called subPPS, aligned to the UTC-PPS (Pulse-Per-Second) but shifted back by half of the window length T and

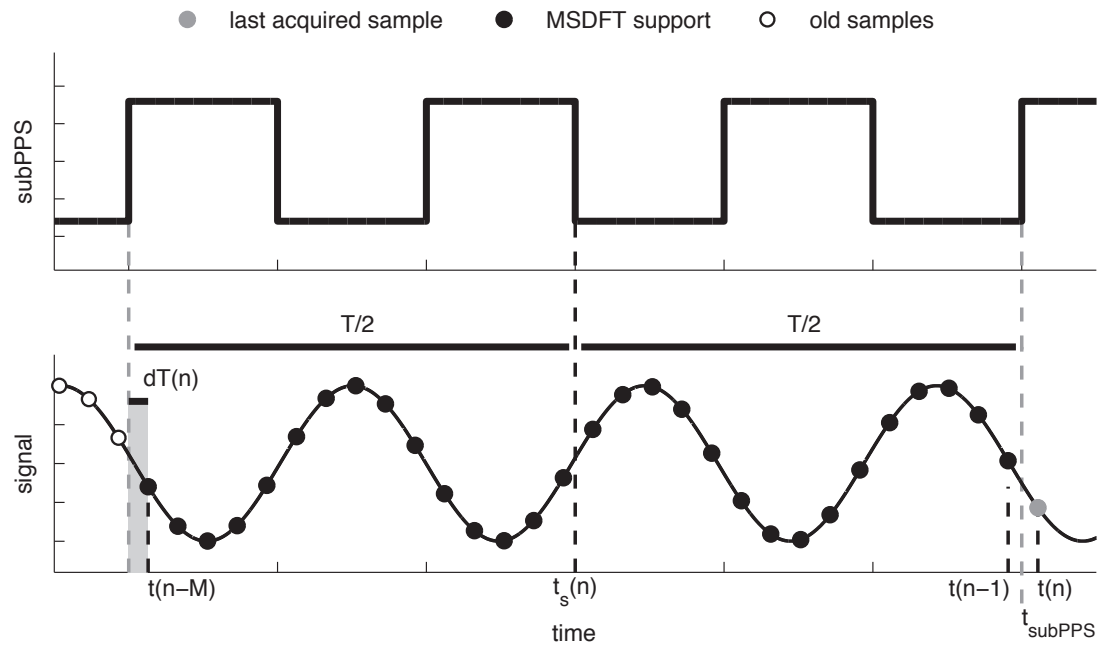


Figure 4.7 – Synchronization of the PMU estimations to the UTC time with a free running clock. A PPS-aligned square waveform triggers the PMU estimations that are compensated for the delay between the first sample of the window $x(n-M)$ and rising time of the subPPS waveform.

characterized by a frequency equal to the PMU reporting rate (see Figure 4.7). The rising edge of the subPPS waveform triggers the i-IpDFT synchrophasor estimation algorithm, that uses the second last MSDFT update (i.e. the one based on the set of samples centered around the reporting time) to provide the most recent PMU estimation.
Unfortunately, if the sampling process is free-running, based on the environmental conditions, the sampling clock will drift and the 1st sample of the window will be rarely aligned to the subPPS (see Figure 4.7). In order to correct the effects of the free-running sampling process, 2 main countermeasure must be taken:

- the time-stamp value, together with the estimated phase, must be compensated for the time difference between the subPPS rising edge and the first sample of the window:

$$\Delta t(n) = t(n-M) - (t_{subPPS} - T) \tag{4.2}$$

  otherwise their accuracy will be proportional to the sampling time T_s (see Figure 4.7);

- in order to improve the frequency (and therefore the phase) estimations, the window length needs to be measured in real time and, as the sampling process drifts, opportunely compensated.

The next sections will discuss about these corrections.

Phase offset compensation

A common problem occurring when a free running clock is used for the signal acquisition refers to the fact that the synchrophasor phase is known with an accuracy that, neglecting the uncertainties due to the synchrophasor estimation algorithm, is correlated to the sampling time T_s. In particular, such an uncertainty corresponds, for F_s=50 kHz and a rated system frequency of 50 Hz, to a bias up to 2π mrad (0.36 deg). In this respect, the algorithm applies a further step on the FPGA level in order to improve the estimation of the synchrophasor phase ψ: since the sampling of $x(t)$ is triggered in correspondence of a rising edge of the subPPS square waveform (see Fig. 4.7), it is possible to freeze the UTC time stamp of the first sample of $x(t)$ and calculate the time delay between the rising edge of the subPPS waveform and the first sample of the window. Based on these consideration the final phase estimation may include the following compensation:

$$\widehat{\psi_c}(n) = \widehat{\psi} + \Delta\varphi \tag{4.3}$$

$$= \widehat{\psi} + 2\pi\widehat{f}\Delta t \tag{4.4}$$

$$= \widehat{\psi} + 2\pi\widehat{f}\,[t(n-M) - t_{subPPS}] \tag{4.5}$$

where $t(n-M)$ and t_{subPPS} are the absolute time of the first sample of the window and of the rising edge of the subPPS square wave respectively.

Free-running Clock Compensation

As mentioned before, another problem refers to the fact that any free running sampling clock (usually implemented with a quartz crystal oscillator) does not run at the exact frequency specified by its data-sheet. On the contrary, it is affected by a small but continuous drift that, if accumulated, may bring to considerable errors in the waveform parameters estimation. Generally the sampling clock drift – usually expressed in units of part per million (ppm) – depends on its quality, the exact power it gets from a DC source, the surrounding temperature and other environmental variables, but also depends on the specific fabrication procedure of the quartz oscillator. Thus, even thought the data-sheets of quartz oscillator declare a maximum clock drift in the order of ±100 ppm, typical values observed during tests run at environment temperature on several devices were equally distributed in the range between ±10 ppm. These specific values correspond to a misestimation of a single period of a 50 kHz sampling clock in the order of ±0.2 ns, that, accumulated over a window of, for instance, N = 3000 samples, may result into a misestimation of the window length in the order of ±0.6 µs. Basically, as we are acquiring portions of waveform that are stretched in one way or another, the computed DFT may be consecutively misinterpreted resulting in non-negligible misestimation of the waveform parameters. In particular, the previously reported maximum error of ±0.6 µs will directly bias the DFT frequency resolution Δf and, consequently affect the estimated frequency $\widehat{f}$ with a maximum error in the order of 5 mHz for a signal at a rated frequency of 50 Hz.

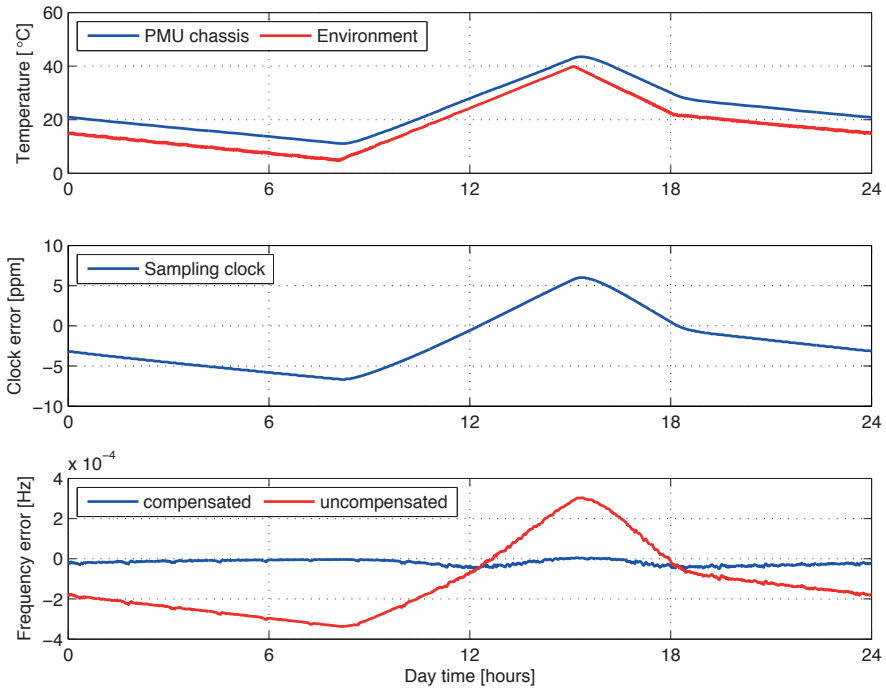


Figure 4.8 – A 24-hours test showing the effects of the compensation of the sampling clock drift.

Since PMUs are inherently equipped with accurate time reference units like GPS, the FPGA clock error ε can be measured in real-time over sufficiently long observation windows (1-10 [sec]) as:

$$\varepsilon_{clock}(n) = \frac{t(n) - t(n-M)}{M \cdot T_s} - 1 \tag{4.6}$$

where $t(n)$ and $t(n-M)$ represent the absolute times of the samples at the end and the beginning of the observation window respectively, M is the window length expressed in equivalent number of samples and t_s is the nominal sampling time. To be noticed that, based on equation (4.6), the FPGA clock error ε is assumed to be negative when $f_s > f_{s,nom}$, positive when $f_s < f_{s,nom}$, where $f_{s,nom}$ is the nominal sampling frequency (i.e. 50 [kHz] in our case). Every time the FPGA clock error is updated, the DFT frequency resolution can be adequately compensated as

$$\Delta f(n) = \Delta f_{nom} \cdot [1 - \varepsilon_{clock}(n)] \tag{4.7}$$

being $\Delta f_{nom} = 1/T$. For ease of implementation, such a correction factor is first measured in the FPGA, then shared with the real-time processor and finally applied before the data are encapsulated in a C37.118-compliant data frame.
As previously mentioned, the sampling clock drift is mainly affected by temperature. In the specific case of PMU applications, the environmental temperature of an electrical substation

Table 4.2 – Values of the parameters used in the ROCOF estimator.

a_1	b_0	b_1	th_1 [Hz/s]	th_2 [Hz/s^2]	th_3 [Hz/s]
-0.5913	0.2043	0.2043	3	25	0.035

is not usually controlled and may largely bias the PMU's performances. In this respect, a dedicated test was designed to prove the proposed approach when the temperature changes according to a typical temperature profile of an electrical substation (i.e. in the range between 5-40 °C). Two different PMU prototypes, both based on the proposed e-IpDFT approach, were installed into a temperature-controlled chamber simulating the above mentioned profile, and the performances with and without the clock error compensation were compared. Fig. 4.8, showing the results collected during a test run over 24 hours, demonstrates that, despite the clock error variations along the day, the proposed approach is capable of compensating for the temperature effects and improving the frequency estimation up to one order of magnitude.

4.4 CPU Resources Allocation

In the adopted design the dual-core ARM processor does not include any time-consuming operation. In particular, as shown in Figure 4.3, the estimated synchrophasors are first retrieved from the FPGA and eventually corrected for the previously measured ADC clock drift. Here the ROCOF is also computed (see Section 4.4.1). Then the estimated values are encapsulated into a C37.118 compliant data frame that is streamed to the external world through the PMU Ethernet adapter. In parallel, a low priority process, verify any eventual requests to change the PMU configuration and reflect these changes by updating the PMU configuration file.
In what follows the analysis will focus on the development of a suitable ROCOF estimator and on the description of the remote PMU configuration.

4.4.1 ROCOF Calculation

The Rate Of Change Of Frequency (ROCOF) can be computed through any finite difference formula for the approximation of the analytical derivative of the estimated frequency. In order to minimize its impact on the ROCOF response time, a classical backward first-order approximation of a first-order derivative was chosen:

$$\dot{f}(n) = \frac{\widehat{f}(n) - \widehat{f}(n-1)}{T_r} \tag{4.8}$$

where $T_r = 1/F_r$, being F_r the PMU reporting rate.
Since finite-difference formula are well known for deteriorating the signal-to-noise ratio (SNR) of the input quantity, equation if (4.8) is adopted to estimate the ROCOF, its values may be degraded well outside the accuracy limits specified by [1] (particularly when the system is in

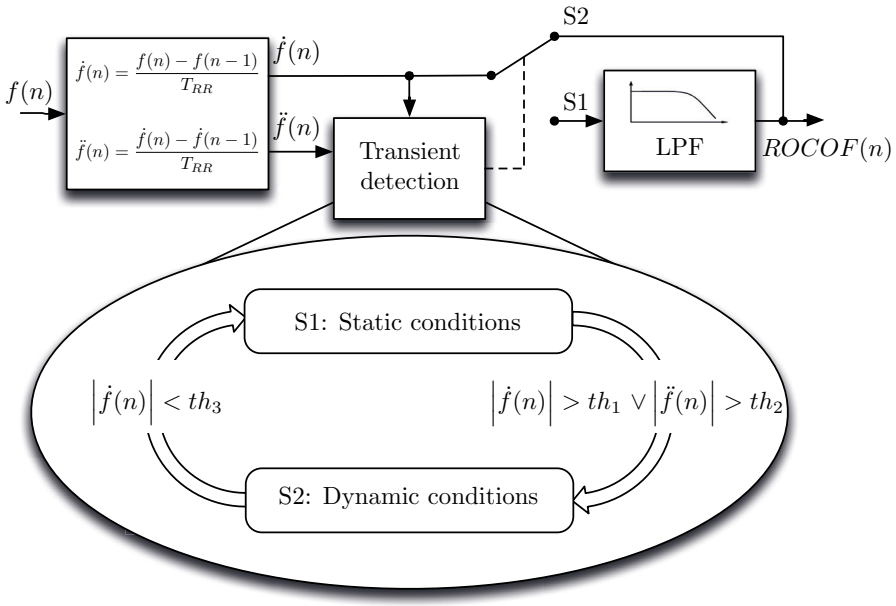


Figure 4.9 – Block scheme of the proposed ROCOF estimator and finite-state machine representation.

steady-state conditions where the IEEE Std. requirements are more demanding). In view of this, the proposed ROCOF estimator is characterized by an additional stage that, based on the detected "state" of the power system, performs the smoothing of the estimated $\dot{f}$ by means of a low-pass filter (LPF). In case of quasi steady-state conditions, the LPF is applied to equation (4.8) and $ROCOF = LPF(\dot{f})$. On the other hand, if the PMU detects dynamic conditions, the smoothing stage is bypassed and the $ROCOF$ is computed according to equation (4.8) only (see Figure 4.9).

Going into details, the detection of a superposed transient to the synchrophasor, is implemented as a finite-state machine characterized by 2 states {S1, S2}, associated to "static" and "dynamic" conditions respectively. The transition between the two states is based on the instantaneous values of the first $\dot{f}(n)$ and second-order derivatives $\ddot{f}(n)$ of the estimated frequency red with respect to the threshold values $\{th_1, th_2, th_3\}$.

On the other hand, the LPF has been implemented as a 1st order IIR (Infinite Impulse Response) LPF that, as known, can be described in terms of the following difference equation:

$$y(n) = b_0 x(n) + b_1 x(n-1) - a_1 y(n-1) \tag{4.9}$$

being x and y the input and output of the LPF and a_i and b_i the feedback and feedforward filter coefficients respectively. The threshold values $\{th_1, th_2, th_3\}$, together with the LPF coefficients $\{a_1, b_0, b_1\}$, have been suitably tuned in to order remove as much as possible the estimation noise, without affecting the transient behavior of the ROCOF. As an example, their values for a reporting frequency of 50 [fps] are given in Table 4.2.

4.4.2 PMU Remote Configuration

In parallel to the FPGA data retrieving, encapsulation and streaming, a low priority process has been designed to remotely configure the PMU. Such a functionality is a necessary, particularly when the PMU configuration process is based on several parameters that defines not only the content of the streamed frames, but also influences the quality and quantity of the PMU measurements.
The current PMU configuration is stored in a configuration file that is formatted according to the JavaScript Object Notation (JSON) format [96] and structured in the following "groups":

- the *Base* group includes all the main PMU parameters specified in the IEEE Std. [18] like the nominal system frequency, reporting rate, PMU ID and station name and allows to configure some of the parameters of the i-IpDFT SE algorithm like set the sampling frequency and the window length;
- the *Communication* group is meant to configure the PMU communication settings, including the streaming protocol (i.e., UDP or TCP), the destination IP address and port;
- the *Sensors* group allows to select the installed ADC modules among a predefined list, configure the measured quantity (i.e. voltage or current) and the bus-bar connection (as known, within a specific substation, a PMU might measure multiple bus-bars) and gives the possibility to compensate for eventual gain and phase transformations generated by the sensors that interface the PMU to the high voltage and current signals;
- The *Phasors* group allows to select, per each bus-bar, which synchrophasors the PMU streams. The user can select both per-phase and sequence phasors;
- The *Analog* group allows to select, per each bus-bar, which analog values the PMU streams (see [18]) among a predefined set of analogs that includes the active, reactive and apparent power together with the power factor;
- The *Digital* group, finally, is meant to configure eventual digital input modules that might be installed in the PMU to check the substation breaker status.

The dual core CPU has been programmed to host a PMU configuration process, in other words a web-service that verifies any request of "configuration change" received by the user and, in case, fetches the current configuration file and publishes its contents on a specific user-friendly interface implemented as an HTML web-page. Here the PMU configuration can be verified and eventually modified by overwriting the existing configuration file with a new one that is derived from the web-page.

5 Metrological Characterization of the Developed PMU Prototype

This chapter presents the metrological characterization of the developed PMU prototype assessed by means of a dedicated PMU calibrator developed in collaboration with the Swiss Federal Institute of Metrology (METAS). The calibrator is based on a National Instrument PXI system and designed to match the more stringent accuracy requirements needed by PMUs expected to operate in ADNs. After presenting the PMU calibrator architecture and the metrological characterization of its components, the PMU performances will be assessed with respect to the testing conditions dictated in the IEEE Std. C37.118 and the characteristic ADNs operating conditions discussed in Chapter 2.

5.1 Metrological Characterization of PMUs

The metrological characterization of PMUs is a process that allows to assess the performances of this kind of devices in terms of synchrophasor estimation accuracies and measurement reporting latencies and, eventually, allows to verify its conformity with the IEEE Std. C37.118 [1, 8] measurement requirements. Such a process is usually composed by two consecutive stages:

- the generation of reference waveforms that emulate typical PMU operating conditions (see for instance the testing conditions dictated by [1]);
- the assessment of the quality of the PMU estimations by comparing them to the "true" parameters of the generated reference signals.

The PMU metrological characterization is typically performed by means of a PMU calibrator, basically a reference signals generator, that is directly connected to a PMU under test to monitor its performances when subjected to various kind of emulated operating conditions. A PMU calibrator operates in a complementary way compared to a PMU and this is reflected

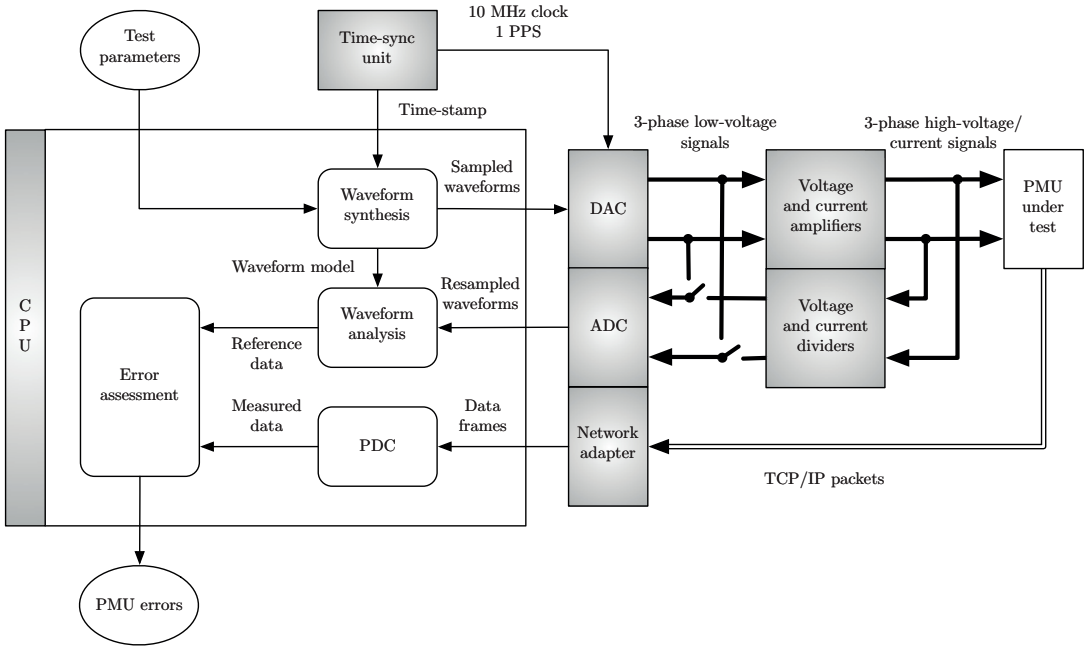


Figure 5.1 – Block scheme illustrating the main hardware (in gray) and software (in white) components of a generic PMU calibrator and highlights their inter-dependencies.

by both the hardware components and software functionalities that it must include. In this respect Figure 5.1 shows the architecture of a generic PMU calibrator by highlighting both the hardware components and software processes. A PMU calibrator must be composed by, at least, the following hardware components:

- A set of *Digital-to-Analog Converters* (DACs) that generate the reference waveforms (single- or three-phase, voltage and/or currents).
- A set of *Analog-to-Digital Converters* (ADC) dedicated to reacquire the generated reference waveforms and monitor the status of the PMU calibrator.
- A *time-sync unit* that mainly serves to discipline the DAC and ADC internal oscillators to an external UTC time-reference to be able to generate stable sinusoidal components also over long periods of time.
- A *central processing unit* that mainly acts as a controller of the other hardware components and performs the final PMU performance assessment.
- Depending on the voltage and/or current range of the A/D converters of the PMU, an *amplification stag*e that transforms the synthesized reference waveforms to voltage and current levels that are suitable to be acquired by the PMU under test.
- Voltage and current *dividers* to transform the high voltage/current signals to levels that can be easily acquired by the ADC.

The operating principles of a PMU calibrator are the following. The user first set the test parameters identifying the reference waveforms to be synthesized. In parallel, the time-sync unit decodes a timing signal (for instance the one disseminated through the GPS system) that is used to discipline the DAC and ADC oscillators to the UTC time-reference. The synthesized samples of the reference waveforms are then generated through the DAC and eventually fed to a set of voltage and current amplifiers that amplify the input signals to voltage and current levels that are more suitable for the PMU ADCs operating ranges. The same waveforms that are acquired by the PMU are also transformed to low voltage levels to be reacquired by the PMU calibrator ADCs. The reacquired samples are then processed by the PMU calibrator according to the adopted testing conditions (i.e., related waveform model) to obtain the "true" reference data. The PMU calibrator also integrates a Phasor Data Concentrator (PDC) that (i) receives the PMU estimations encapsulated in C37.118 data frames, (ii) extracts the measurement data encapsulated in the PMU data frames and (iii) time-aligns them with the reference data. Finally another process extracts the time-aligned information and compares the reference and measured data to obtain the PMU errors and, eventually, determine the PMU compliancy to the IEEE Std. C37.118.

It is evident that the biggest challenge when metrologically characterizing a PMU is related to the possibility of knowing instantaneously the "true" parameters of the generated reference waveforms. As already discussed along this thesis (see Section 1.3.3), this assumption is ideal as the reference waveforms, thus their parameters, are characterized by an uncertainty corresponding to the uncertainty associated to the hardware components included in the forward chain of the PMU calibrator (namely the time-sync unit, the DAC and the voltage/current amplifiers).

In a first approximation, the PMU calibrator characteristic uncertainty can be derived from the datasheet of each component within the forward calibration chain, by combining the characteristic amplitude and time (i.e., phase) accuracy of each component into an equivalent global TVE uncertainty (see Section 1.3.3). This, in order to correctly interpret the PMU calibration results, must necessarily be, at least, one order of magnitude lower than the one of the PMU under test.

Even though such an approach can be adopted to calibrate PMUs operating in transmission networks, it is not suitable for the metrological assessment of PMUs designed for distribution networks applications. Indeed, as already analyzed in Chapter 2, due to the short line length and reduced power flows, PMUs operating at this level must be capable of measuring very small magnitude and phase angle differences between nodal voltage and line current phasors at the estremities of a transmission line, in order to correctly monitor the power system where they have been deployed[1]. In particular, the estimation of phase angle differences in the order of few tens of millidegrees is the biggest challenge.

This characteristic must necessarily be reflected by PMU calibrators that, in order to be capable of metrologically evaluating the performances of this kind of devices, must be characterized by extremely reduced amplitude and time uncertainties. In this respect, Table 5.1 shows

[1] In Section 2.2 the TVE limit of 0.01% has been adopted to determine the PMU compliancy to operate in distribution networks.

Table 5.1 – Maximum magnitude, phase and timing accuracy for different values of TVE (1% TVE is the IEEE Std. C37.118 typical limit). The table shows a 5 fold improvement at each line.

TVE [%]	Mag. Error [ppm]	Phase Error [mrad]	Phase Error [deg]	Time Error [µs]
1	10,000	10	0.57	32
0.2	2,000	2	0.11	6.4
0.04	400	0.4	0.022	1.3
0.008	80	0.08	0.0046	0.25
0.0016	16	0.016	0.00092	0.050

the maximum allowable amplitude and time errors for different values of TVE and a power system frequency of 50 Hz [97]. Recalling that PMU calibrators must be characterized by an uncertainty that is, at least, ten times lower than the one of the PMU under test, the metrological assessment of PMUs for DN applications becomes a remarkable technical and scientific challenge. In this respect, relying on the datasheet values to determine the PMU calibrator characteristic accuracy is not a valuable solution as they were not conceived to go to such a level of details. Additionally, most of the times datasheets might depict a "worst-case" scenario as they are typically compiled by adopting a conservative approach.
In this respect, a more elegant and precise approach refers to the combination of:

- high-accuracy hardware components that are metrologically characterized, beyond their datasheet values, with respect to the usual operating conditions of PMU calibrators;
- an active calibration feedback chain that constantly monitor the quality of the generated reference waveforms and eventually compensates for the instantaneous variations of the reference parameters due to, for instance change in the environmental conditions.

5.2 The EPFL-METAS PMU calibrator

A calibrator for PMUs operating in DNs was designed, according to the considerations made in the previous Section, in collaboration with the Swiss Federal Institute of Metrology (METAS) and in the context of the European Metrology Research Program (EMRP), Project ENG04 "Metrology for Smart Electrical Grids". The aim of this research is the development of a metrological grade instrument suitable for the full certification or verification of PMUs against and beyond the IEEE C37.118.1 testing conditions.
The architecture of the PMU calibrator follows the guidelines given in the previous Section and reflects what shown in Figure 5.1 in terms of both hardware and software components and their inter-dependencies. The system is depicted in Figure 5.2 and based on a National Instruments PXI (PCI eXtensions for Instrumentation) 1042Q chassis [98] in which the following modules are plugged:

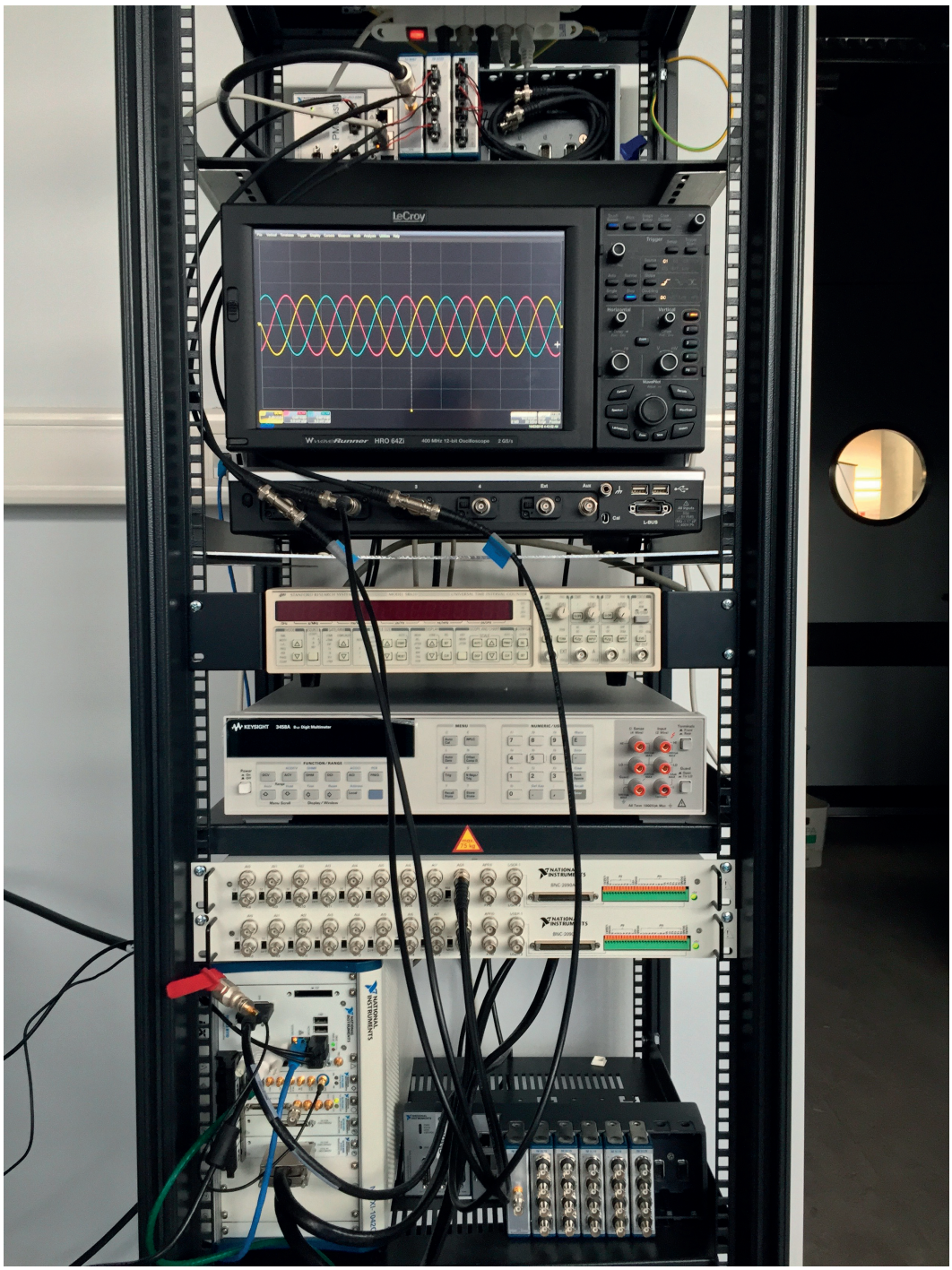


Figure 5.2 – The PMU calibrator developed in collaboration with the Federal Institute of Metrology Switzerland (METAS). From top the following components are visible: (i) the PMU under test, (ii) an oscilloscope to verify the quality of the reference waveforms, (iii) the FS725 10 MHz Rb frequency standard, (iv) the high-precision digital voltmeter HP 3458A, (v) the DAC and ADC extensions and (vi) the PXI 1042Q chassis (on the left).

- a NI PXI-8110 high-performance Intel Core 2 Quad Q9100-based embedded controller [99] that controls the other connected boards;
- a NI PXI-6682 timing and synchronization module [100] that provides absolute-time information to the whole chassis by synchronizing it to a time-reference that can be either provided by GPS, IRIG-B, IEEE 1588 (PTPv2) or PPS (see Section 1.2 for further details on the available time-dissemination technologies);
- a set of NI PXI-6289 high accuracy data acquisition (DAQ) and generation (low-voltage ($\pm$10 [V]) boards [101] that acts both as DACs (signal generation) and ADCs (signal acquisition);

In addition to this, the following external units are connected to the PXI chassis:

- a GPS-disciplined FS725 10 MHz Rb frequency standard by Standford Research Systems [102] that is used as time-reference to discipline both the DAC and ADC sampling process;
- a high-precision digital voltmeter HP 3458A [103] that monitors in real-time the RMS variations of the generated reference waveforms.

The NI PXI-6682 synchronization board receives absolute time information from the GPS system with an accuracy lower than 100 ns. This is used to time-stamp both the generated and reacquired waveform samples and to measure the PMU measurement reporting latency. Furthermore, in order to reduce the timing uncertainty contribution, the time-sync unit has been designed to receive an ultra accurate and stable time-reference signal generated outside of the PXI platform. This, in the best case, can be the time-reference provided by the UTC-CH system, i.e., the official UTC-time reference in Switzerland that is generated and disseminated only within the METAS laboratories through coaxial cables (nevertheless, future UTC-CH dissemination through PTPv3 is envisaged). Alternatively it can be provided by an accurate GPS-synchronized atomic clock, like the GPS-disciplined FS725 10 MHz Rb frequency standard by Standford Research Systems, that combines the long-term stability of GPS with the short and medium term stability of an atomic oscillator.
The NI PXI-6682 board receives the pulse-per-second (PPS) signal provided by any of the two time references and disciplines a 10 MHz clock that is distributed on the PXI backplane and shared with every other PXI module with a skew of less than 250 ps. In particular, such a time-reference synchronizes the sampling process of both the DACs and ADCs that are embedded in the PXI-6289 board. The ADC generates the pre-synthesized signal reference waveforms with a sampling rate of 500 kS/s that allows to limit the harmonic distortion of the reference waveforms and to avoid aliasing problems also when the voltage and current amplifiers are bypassed and the PMU is fed with low-voltage signals[2] ($\pm$10 [V]). The DACs on the PXI-6289 have a 16-bits resolution and an amplitude accuracy, declared by the manufacturer, of 1540

[2] This is only valid for PMUs characterized by sampling rates of few tens of kHz.

μV (on the ±10 V range).
For the time being the proposed calibrator does not include yet any voltage and current amplifier. As a consequence the low-voltage reference waveforms are directly applied to the PMU under test simplifying considerably the calibration architecture and logic. This choice is related to the difficulty in finding industrial-grade amplifiers that are matching the amplitude and phase uncertainty requirements that have been set for calibrators of PMUs that will operate in DNs. In this respect, the design of ad-hoc voltage and current amplifiers and dividers is a necessary and time-consuming process that has not been concluded yet. Nevertheless it is worth observing that the majority of modern sensors installed in DNs are characterized by low-voltage outputs (typically in the ±10 V range). Therefore, for PMUs designed to be interfaced with this kind of sensors, there is no need to further amplify the reference signals. The reference waveforms are simultaneously acquired by the PMU and the ADCs of the NI PXI-6289 board, that are characterized by an 18-bits resolution and an amplitude accuracy, declared by the manufacturer, of 980 μV (±10 V range). Nevertheless, as it will be demonstrated later, such an uncertainty can be metrologically characterized before the PMU calibration process and eventually compensated to improve the PMU calibration overall uncertainty. These reacquired signals are then processed so that they can directly be compared with the data reported by the PMU under test. In this respect the waveform parameters are estimated using a least square fitting technique applied to the time stamped samples, which has been first presented in [97]. The fitting permits to establish the actual parameters such as magnitude, phase, frequency and ROCOF. The fitting is often facilitated by the fact that some parameters such as modulation frequency do not require extraction as the highly accurate time synchronization ensures their correctness. For steady state compliance tests, the fitting uses a linear model with one or two sine waves of known frequency. However, for dynamic tests, the signal may contain modulation forcing the use of iterative methods (nonlinear). However, the convergence is generally fast as the initial conditions are those used in generated waveform (synthetic data). The small differences between the acquired waveform and those generated are caused primarily by the frequency response of the amplifiers.
As already discussed in the previous section, the ability of a PMU calibrator to metrologically characterize PMUs designed for DN applications is determined by the possibility of metrologically characterizing the magnitude and time (i.e., phase) uncertainties introduced by each hardware component composing the PMU calibrator. In this respect, in what follows the measured time/phase and amplitude uncertainties will be presented together with a description of the adopted methodology.

5.2.1 Metrological Characterization of the PMU Calibrator

The characteristic uncertainty of a PMU calibrator is usually expressed in terms of an equivalent TVE but can be decoupled in terms of both phase and amplitude uncertainties in order to better understand the various contribution of the different hardware components. In particular the phase error is influenced both by time-synchronization and phase uncertainties. The former is caused by the misalignment of the master clock with UTC whereas the latter

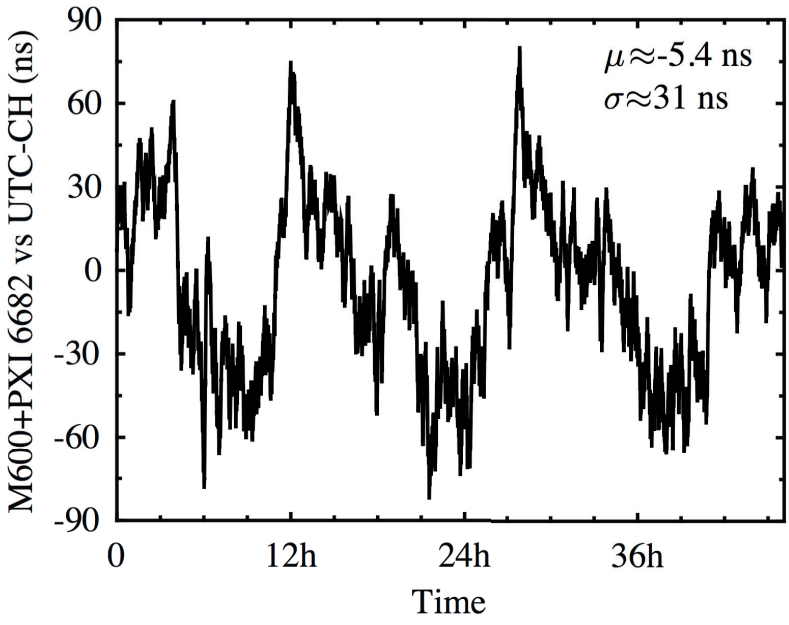
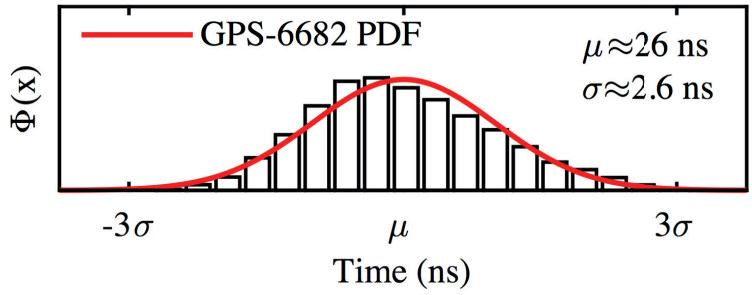


Figure 5.3 – A 24 hours test showing the combined uncertainty of two arbitrary GPS receivers, the Meinberg LANTIME M600 and the PXI-6682, when referenced to the UTC-CH.

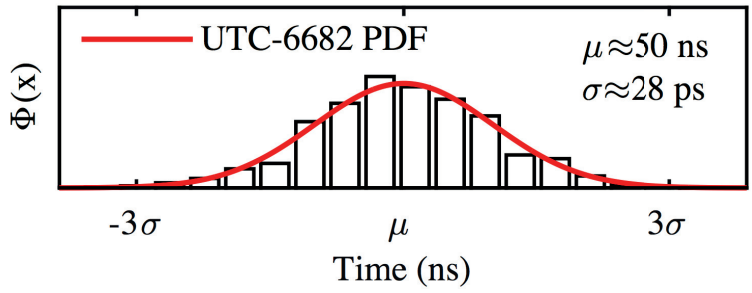
is introduced by the various phase shift and delays in the hardware components of the PMU calibrator. On the other hand, the magnitude error drift is primarily caused by the resistors values of the hardware components that change over time and with temperature.
In what follows the above mentioned uncertainties are carefully evaluated and the characteristic uncertainty of the developed PMU calibrator will be given in terms of an equivalent TVE.

Time-synchronization Uncertainty

The most advanced PMU calibrators that are nowadays available (see [104] for instance) are time aligned to UTC via the Global Position System (GPS). As a consequence, when a PMU is being characterized with such a calibrator, two GPS-receivers are actually involved: the one that synchronizes the PMU calibrator and the one embedded in the PMU itself. Even though, the two GPS-receivers are physically very close and, in a first approximation, they receive the same GPS signal, they are not synchronized together. This is mainly due to the different synchronization techniques that are adopted within each one of the GPS receiver, that, generally, might come from different vendors and/or developers.
In general the relative uncertainties of the two involved GPS-receivers (i.e., the one of the PMU and the one of the PMU calibrator) could add up together distorting the reliability of the calibration. Figure 5.3 shows an example of the combined uncertainty of two arbitrary GPS-receivers (Meinberg LANTIME M600 and a PXI-6682) with respect to UTC-CH generated



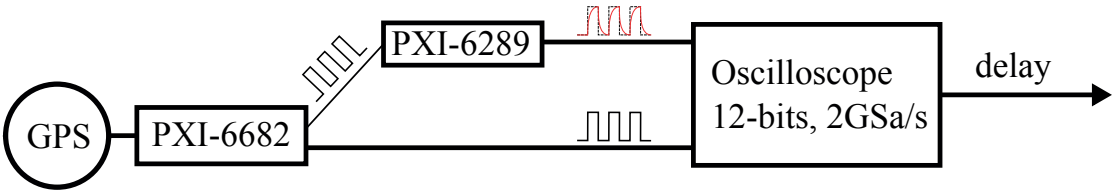
(a)



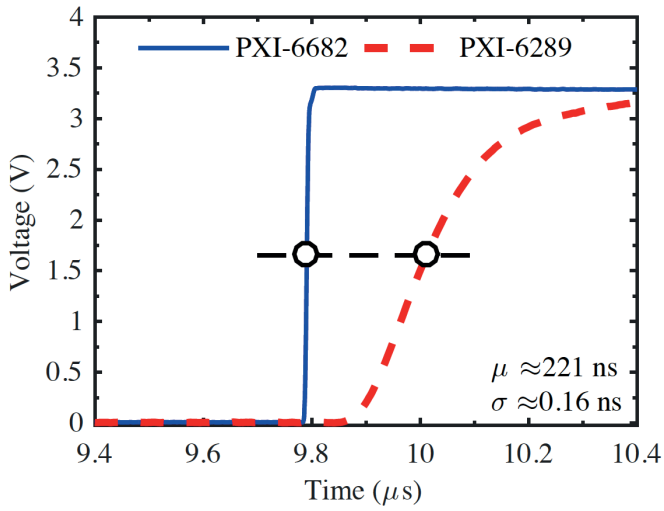
(b)

Figure 5.4 – Probability density function of the timing uncertainty of the PXI-6682 disciplined by GPS (a) and UTC (b). The PPS signal, routed out from the PXI-6682, is compared against the PPS signal of the UTC-CH.

by METAS. The combined uncertainty of the two GPS-receivers follows a normal distribution characterized by $\mu \approx$-5 ns and $\sigma \approx$ 30 ns. Therefore, the total timing uncertainty caused by the two GPS-receivers corresponds to approximately 30 µrad ($\pm 3\sigma$).
A better phase accuracy can therefore be achieved by substituting the GPS-receiver of the PMU calibrator with a more accurate master clock. In this respect the following test quantifies such an improvement by comparing the common approach where the master clock is represented by the GPS signal with the proposed solution that adopts the UTC-CH.
In both cases, the PXI-6682 is disciplined by the master clock and generates a PPS signal. The PPS signal, routed out from the PXI-6682, is then compared against the PPS signal of the UTC-CH (UTC-PPS) through a Universal Time Interval Counter SR620 [105]. As shown in Figure 5.4, the short-term accuracy of the PXI-6682 output referred to UTC-CH follows a normal distribution. When the PXI-6682 is disciplined using as a master clock the GPS signal, the short-term accuracy of the PXI-6682 is about 26 ns. Instead, when the PXI-6682 is directly disciplined by UTC-CH signal, the short-term accuracy that actively contributes to the TVE of the PMU calibrator improves of circa 100 times. The timing uncertainty introduced by the PXI-6682 when disciplined through the UTC-CH has been estimated to circa ±81 ps (this number refers to the $\pm 3\sigma$ of the distribution shown in Figure 5.4). For a 50 Hz reference signal,



(a)



(b)

Figure 5.5 – The adopted setup to metrologically characterize the delay and jitters introduced by the DAC (a) and the characterization of the delay between the PXI-6682 and the PXI-6289 board (b) that has been quantified in the order of 221 ± 0.6 ns.

this uncertainty corresponds to 25 nrad.

Phase Uncertainty

An inaccurate synchronization of the hardware components is translated into a phase error in the reference waveforms. In order to quantify the total phase error of the system, a metrological characterization of the DAC is necessary.
In this respect, in what follows the jitters measurements of the DACs are reported and commented. A sketch of the characterization method is shown in Figure 5.5a. Using the GPS-PPS as a master clock, we have routed out from the PXI-6682 a clock frequency of 100 kHz. Then, we have generated with the PXI-6289 a square waveform of frequency 100 kHz. The sampling rate of the PXI-6289 has been set to 1 MSa/s. Thus, we have acquired 2000 periods of the two waveforms using a high-resolution oscilloscope LeCroy Hro G4Zi (12-bits, 2 GSa/s, clock accuracy of 1.5 ppm and trigger jitter ≤ 6 ps). Figure 5.5b shows an example of the two acquired waveforms. As it can be observed, the output waveform of the PXI-6289 (dashed red line in Figure Figure 5.5b) is smoothed due to the effect of low-pass filters on the PXI module.
The delay between the PXI-6682 and the PXI-6289 is defined as the time difference between

the values reached by the two signals in correspondence of 50% the maximum amplitude. The delay between PXI-6682 and PXI-6289 follows a normal distribution characterized by $\mu \approx 221$ ns and $\sigma \approx 0.16$ ns. The PXI-6289 has a systematic delay of 221 ns, which can be easily compensated, and a random error of 0.2 ns that actively contributes to the TVE of the PMU calibrator. It is worth observing that the oscilloscope used to quantify the delay has a vertical accuracy of 0.5% referred to the full scale (±5 V in our case). In order to assess the consistency of the method, we have inferred the distribution of the delay for the different magnitude thresholds of 0.1%, 0.2% and 0.5%. The systematic delay varies accordingly whereas, considering the errors introduced by the oscilloscope, the random error is constant. The synchronization uncertainty introduced by the PXI-6289 can be estimated in $\pm 3\sigma$, circa±0.6 ns (0.2 μrad).
The same results have been confirmed using the method reported in Section 5.2.1. The output of the PXI-6289 was compared with the PXI-6682 though the Universal Time Interval Counter SR620. The master clock was the GPS signal, the sampling rate was set to 500 kSa/s (nominal sampling rate of the calibrator) and the signal frequency was 50 Hz.

Magnitude Uncertainty

While the phase error can be characterized at the time of design, the magnitude accuracy is difficult to maintain over time and over a given temperature range with an accuracy of about 100 ppm. The magnitude accuracy drift is primarily caused by the ADCs that tend to be sensitive to the temperature. To circumvent this problem, the calibrator is recalibrated between measurements. This is achieved with the usage of a high precision digital voltmeter HP 3458A [103]. This multi-meter has a DC accuracy of up to 8.5 digits and is based on an integrating ADC. However, precision AC measurement can also be made in the DC mode [106]. This instrument is also characterized by a very good 90 days stability and a low temperature coefficient.
A single HP 3458A is configured to calibrate all the three voltage channels between every sub-test of the PMU calibration process. Indeed, between two measurements, the calibrator is configured to continuously generate a signal at nominal values to the PMU under test. During this time, the signal reference waveforms are applied to the HP 3458A and are measured with an accuracy of 100 ppm. The data generated by the DACs in the PMU calibrator are then adjusted based on these measurements. At the moment, since the output range of the calibrator is ±10 V, a maximum uncertainty of 100 ppm corresponds to a global magnitude uncertainty of the calibrator of 0.01%.

5.2.2 Global uncertainty of the PMU calibrator

In the previous Sections a novel methodology to assess the characteristic uncertainty of a PMU calibrator has been proposed. Such an approach is based on the metrological characterization of each hardware component of the calibrator and to an active calibration feedback chain that constantly monitor the quality of the generated reference waveforms.
The uncertainty associated to the time-synchronization has been quantified in ±81 ps. In

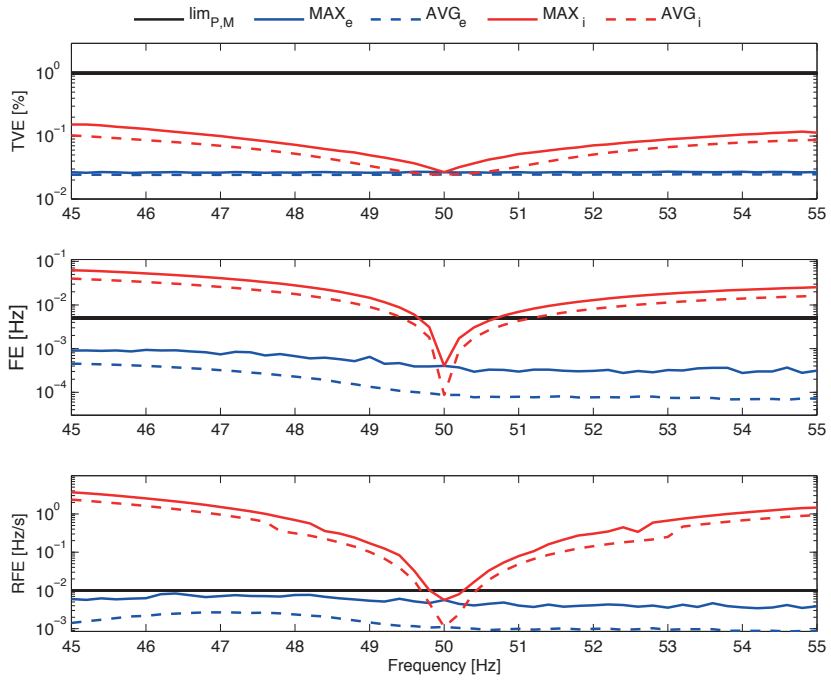
other words it has been reduced by at least 3 orders of magnitude compared to the time-synchronization performances of standard PMU calibrators that adopt the GPS system as a timing reference.
Similarly, the phase uncertainty associated to both DACs and ADCs has been quantified in ±0.6 ns. Finally, by adopting an high-precision voltmeter, we can trust the amplitude calibration results up to the characteristic accuracy of such a device. This can be quantified in 100 ppm. Consequently, the combined timing and synchronization uncertainty of the proposed PMU calibrator are in the order of 1 ns that correspond to a phase error, at 50 Hz lower than 500 nanoradians. With such a low phase uncertainty, the 100 ppm amplitude uncertainty prevails when determining the TVE. Therefore, the proposed calibrator system has an estimated TVE of around 0.01% referred to steady-state conditions. This uncertainty should allow the metrological characterization of the majority of the available commercial PMUs.

5.3 Experimental Verification of the IEEE Std. C37.118 Compliance

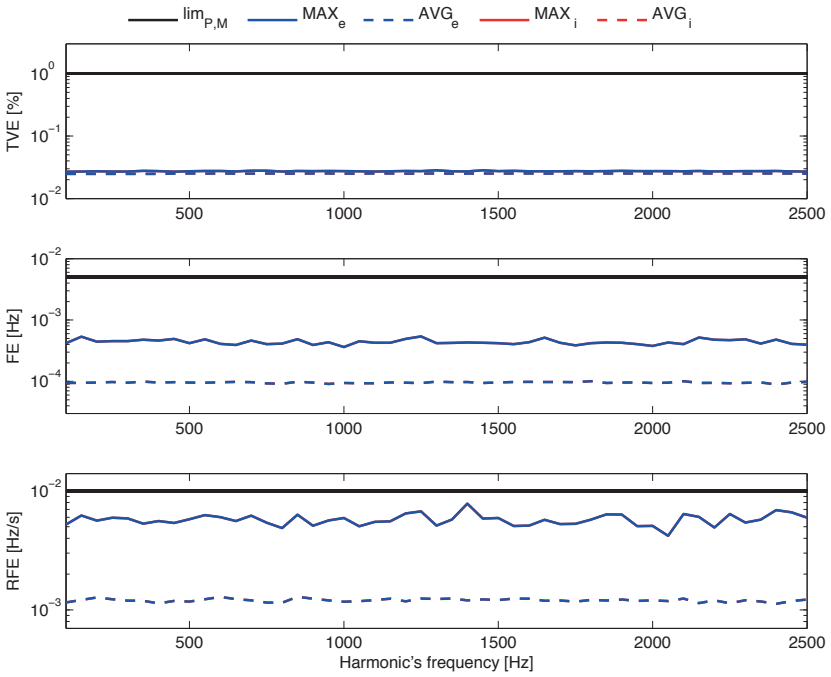
The experimental verification of the IEEE Std. C37.118 Compliance has been carried out using the PMU calibrator presented in the previous Section. Every test described in [1], for both static and dynamic conditions, has been implemented. For the sake of brevity, the experimental results make reference to a PMU configured with a nominal frequency of 50 [Hz] and a reporting rate of 50 frames per second and equipped with 24-bits Delta-Sigma A/D converters characterized by a nominal voltage of 300 V_{RMS} (see Section 4.2.3). As a consequence only the 3% of the PMU ADC input range has been tested, making the presented metrological characterization a “worst case” scenario as larger signals would only reduce the quantization error at the A/D converters output resulting in better performances of the device.
The accuracy assessment presented in this Section compares the performances of the proposed i-IpDFT algorithm when deployed in the adopted PMU hardware (see Section 4) with (in blue) and without (in red) the iterative compensation of the effects of the spectral interference. In other words the red line quantify the performances of a standard IpDFT approach. The errors are shown together with the IEEE Std. [1] accuracy limits and expressed in terms of the standard quantities defined in [1], i.e. the Total Vector Error (TVE), the Frequency Error (FE), the Rate of Frequency Error (RFE) and, for step tests only, the PMU Response Time (RT). In every figure the TVE, FE and RFE, together with the related class P and M accuracy limits, are shown using a logarithmic scale and are computed over a 20 s window in agreement with the IEEE Std. [1] guidelines. Their behavior is described in terms of their maximum and average values apart from step and frequency ramp tests, where the errors are instantaneous.

5.3.1 Steady-state Tests

With reference to steady state conditions, two cases have been analyzed as requested by [1]: (i) single-tone signals characterized by a constant frequency in the range $f_0 \pm 5$ [Hz] (see Figure 5.6a) and (ii) distorted signals characterized by a 10% single harmonic superposed to the nominal frequency tone (see Figure 5.6b) in the frequency range between 100 and 2500 [Hz]. The errors are reported as a function of the nominal frequency and the harmonic component frequency for single tone and distorted signals respectively.
As it can be observed, in the case of the proposed i-IpDFT approach, the TVE, FE and RFE are extremely flat and almost two orders of magnitude below the required limits. They are not affected neither by the nominal frequency of the signal (see Figure 5.6a), nor by the presence or by the order of the superposed harmonic component (see Figure 5.6b).
On the other hand, with the classical IpDFT approach, the performances of the PMU are largely biased by the nominal frequency of the signal. In particular, the effects of the spectral interference are visible when the nominal frequency of the signal deviates from 50 [Hz] and, therefore, the effects of spectral leakage are more significant (see particularly FE and RFE plots of Figure 5.6a). Concerning the case of distorted signals, the performance of the classical IpDFT algorithm are instead comparable to the proposed i-IpDFT approach as the effects of leakage are practically negligible.
As known, the latest version of the IEEE Std. C37.118.1-2011 [1] has introduced, for M-class PMUs only, a challenging "Out of band Interference" test, aimed at verifying the PMU capability to reject inter-harmonics signals. This specific test introduces an additional spectrum tone that, due to spectral leakage, interferes with the main spectrum tone and corrupts considerably the estimations provided by the i-IpDFT algorithm. As a consequence, the proposed i-IpDFT algorithm cannot be compliant to the IEEE Std. limits for this test, as it has been conceived to compensate for the spectral leakage produced by the negative spectrum image of the main spectrum tone only. In this respect the performances of the i-IpDFT approach in the case of out-of band interfering signals, are similar to those of a classical IpDFT algorithm as the one illustrated in [54].



(a)



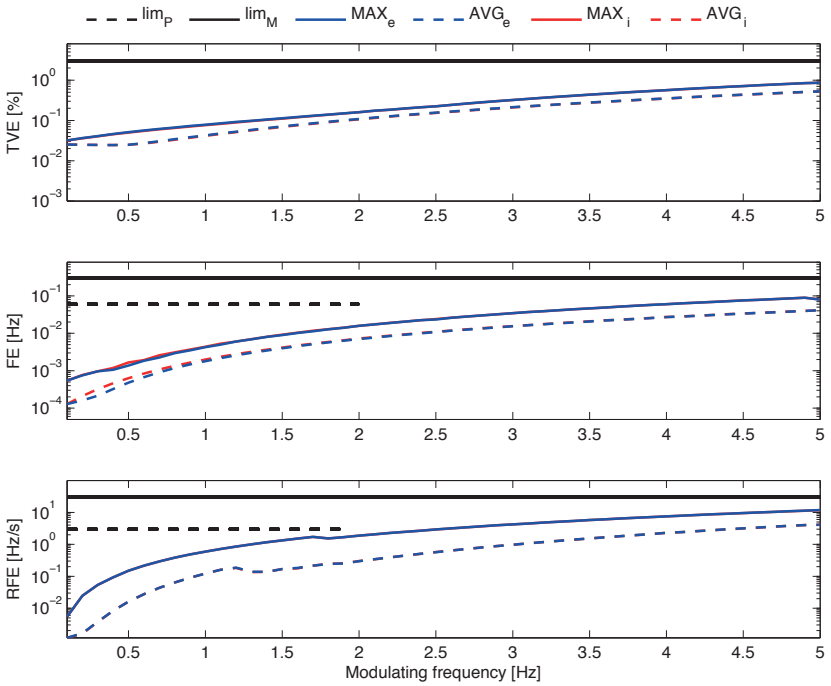
(b)

Figure 5.6 – PMU performances with respect to static tests with single-tone (a) and multi-tone signals (b). Subscript "e" (blue traces) and "i" (red-traces) identify the errors of the i-IpDFT and the classical IpDFT algorithms respectively.

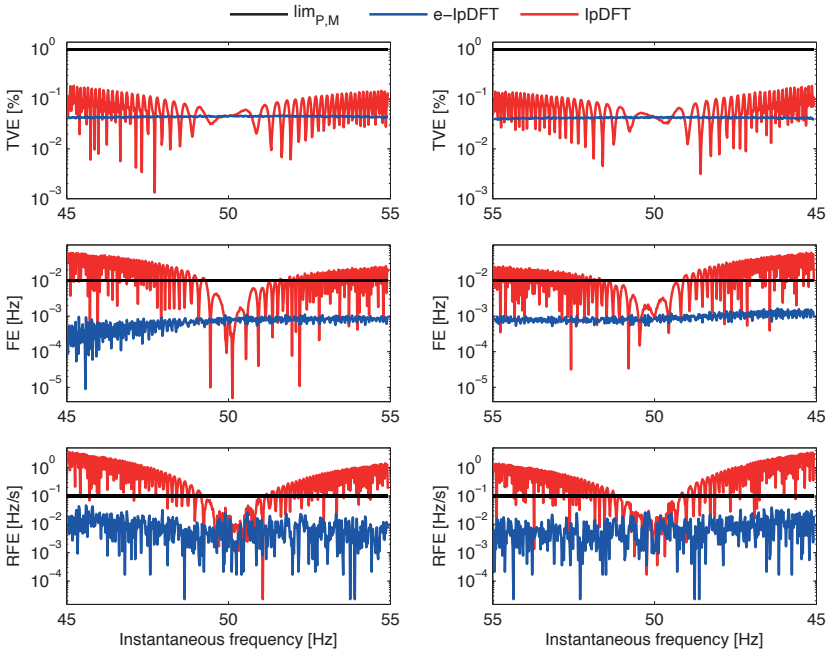
5.3.2 Dynamic Tests

Concerning dynamic conditions, the reference signal generator has been programmed, according to the tests defined in [1], to generate single-tone signals characterized by (a) combined phase and amplitude modulations, (b) frequency-sweep and (c) amplitude and phase steps.
As for (a), a set of reference signals characterized by modulating frequencies in the range between 0.1 and 5 Hz, with frequency steps of 0.1 [Hz], were synthesized and applied at the PMU inputs[3]. Fig 5.7a shows the corresponding estimation errors and highlights the different limits and modulating frequency ranges for classes P and M respectively. In this case the errors of the classical IpDFT and the proposed i-IpDFT are comparable and, despite a worsening of the performances with higher modulating frequencies, the PMU demonstrates to perform well within the IEEE Std. requirements.
Concerning (b), the frequency has been linearly varied in the range between 50 and 55 Hz (positive ramp, see Figure 5.7b, left) and 50 and 45 Hz (negative ramp, see Figure 5.7b, right) at a rate of ±1 Hz/s. It can be observed that the performances of the proposed i-IpDFT algorithm, here reported as a function of the instantaneous frequency, are comparable with those assessed with steady-state single-tone signals and well within the limits. In the case of the IpDFT algorithm instead, the same behavior observed in Figure 5.6a is visible: when the instantaneous frequency deviates from the rated one, the PMU errors increase exceeding eventually the IEEE Std. limits.
Finally, regarding (c), reference signals characterized by positive and negative steps applied to amplitude (±10% of the nominal voltage, see Figures 5.8a and 5.8b) and phase (±10 deg, see Figures 5.9a and 5.9b) were generated. For a more accurate assessment of the PMU response time, the equivalent oversampling approach proposed in [1] using 50 subtests was adopted. Every Figure shows the TVE, FE and RFE profiles during the step change as a function of measured response time. As expected the performances of the classical IpDFT and the proposed i-IpDFT approach are the same, as the proposed spectral interference compensation scheme does not affect the response time performances of the i-IpDFT algorithm. The experimental results demonstrate that, after an unavoidable initial synchrophasor misestimation, the PMU errors always return below the required accuracy limits within the allowed response time [1] for both classes P and M.

[3] To be noticed that for class P these tests have to cover the range of modulating frequencies between 0.1 and 2 Hz whilst, for class M, the modulating frequency has to be increased up to 5 Hz but with larger accuracy requirements.

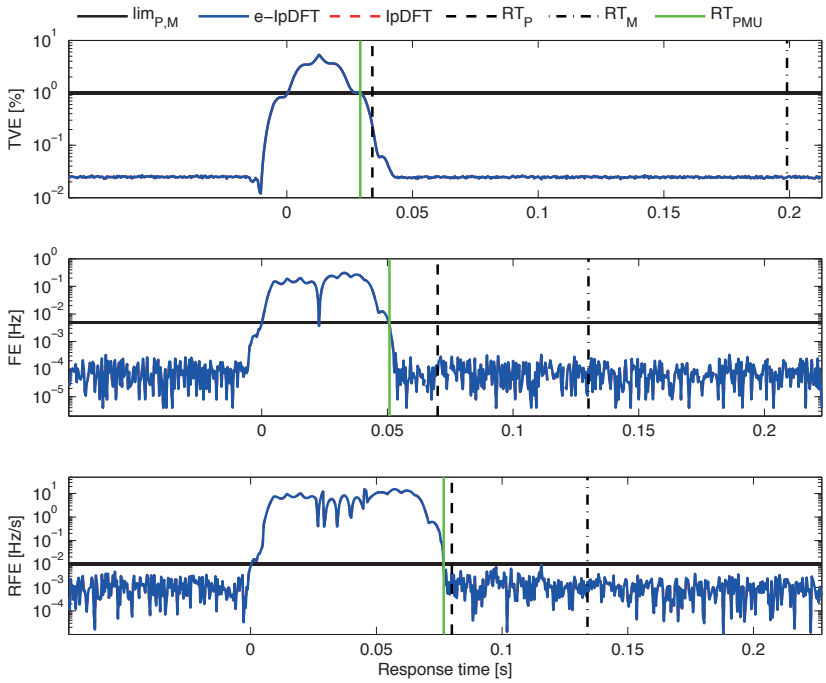


(a)

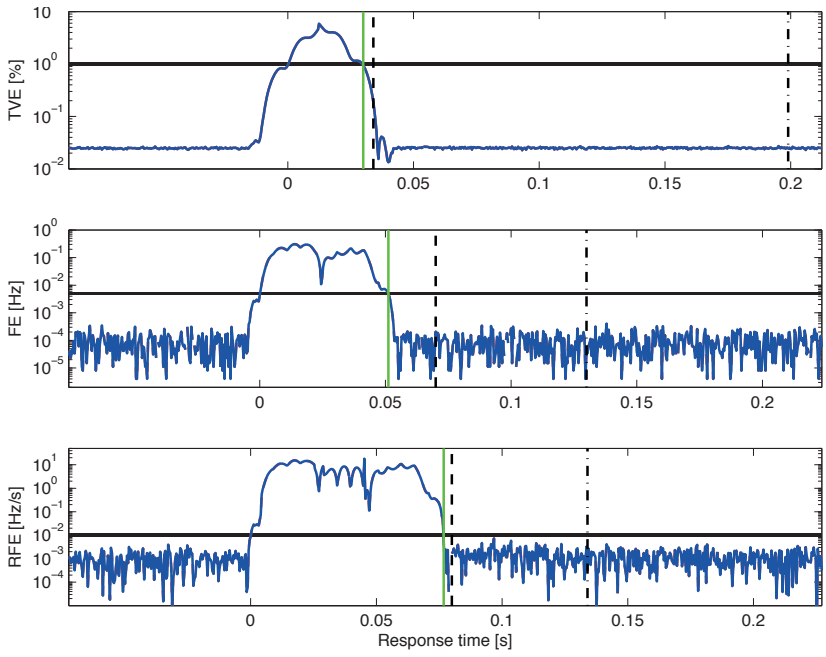


(b)

Figure 5.7 – PMU performances with respect to dynamic tests with combined amplitude and phase modulation (a) and with positive (left) and negative (right) frequency ramp (b). Subscript “e” (blue traces) and “i” (red-traces) identify the errors of the i-IpDFT and the classical IpDFT algorithms respectively.

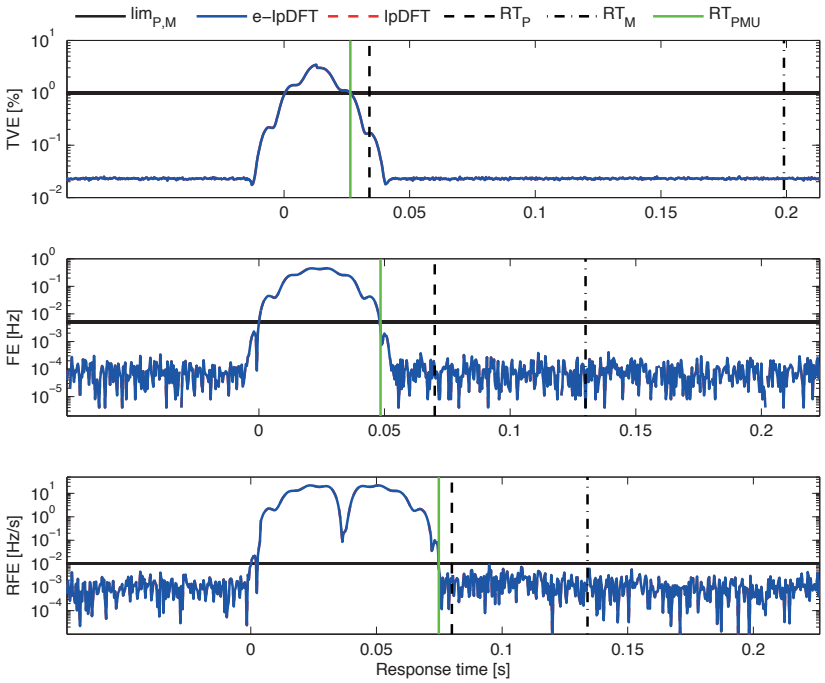


(a)

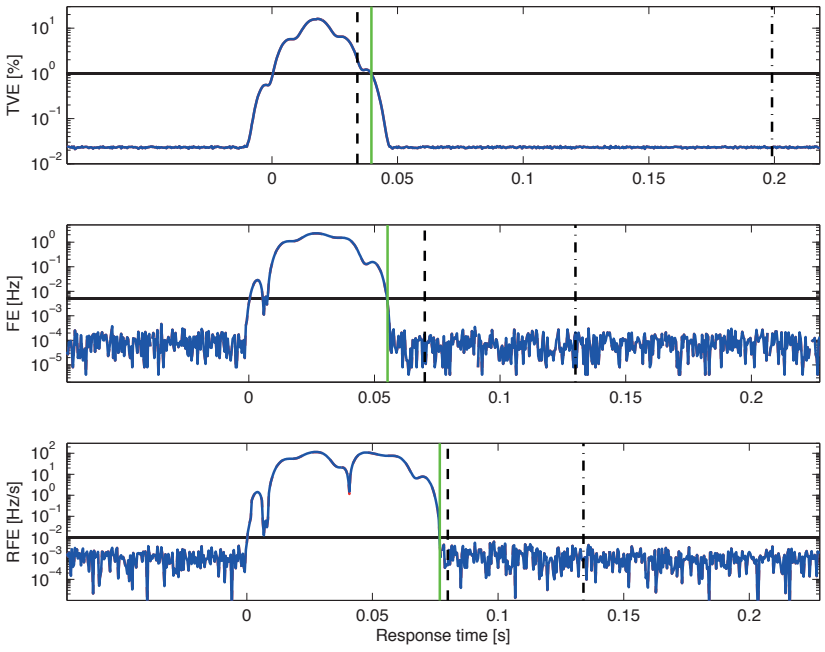


(b)

Figure 5.8 – PMU performances with respect to dynamic tests with positive (a) and negative (b) amplitude steps. Time $t = 0$ corresponds to the moment when the estimated quantity exceeds the IEEE Std. limits. The PMU response time is highlighted in green and compared to the IEEE Std. limits.



(a)



(b)

Figure 5.9 – PMU performances with respect to dynamic tests with positive (a) and negative (b) phase steps. Time $t = 0$ corresponds to the moment when the estimated quantity exceeds the IEEE Std. limits. The PMU response time is highlighted in green and compared to the IEEE Std. limits.

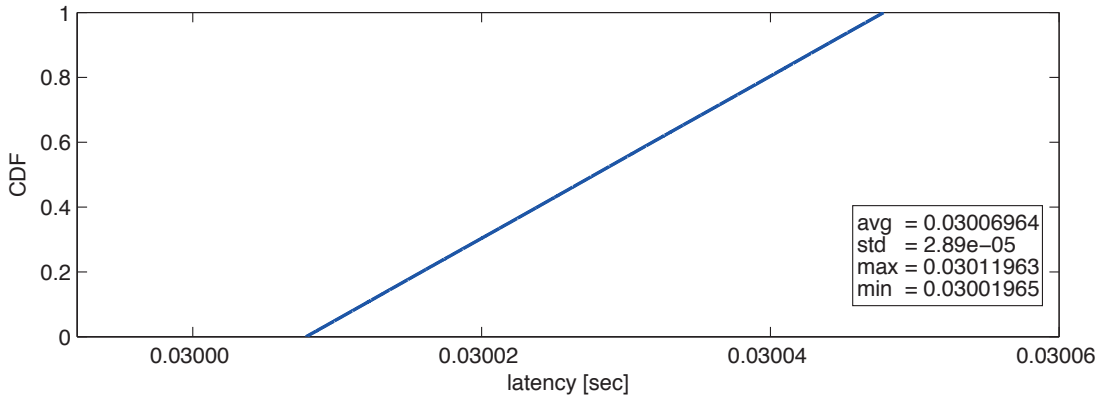


Figure 5.10 – Cumulative distribution function of the measurement reporting latencies for the proposed i-IpDFT algorithm.

5.3.3 Measurement Reporting Latency

The measurement reporting latency is defined as the time-delay from when an event occurs in the power system to the time that it is reported in the data and can be computed as the time interval between the data time-stamp and the time when the data becomes available to the PMU outputs (see Section 1.3.3).
Figure 5.10 shows the cumulative distribution function, computed over 10,000 consecutive estimations, of the measured latencies of the developed PMU prototype that was running at a reporting rate of 50 estimations per seconds (i.e., the test covers a time interval of more than 3 minutes). As it can be noticed the distribution of the measurement reporting latencies is uniform with an average value of 0.030069 sThis time is assessed using the GPS time reference available on the PMU FPGA and shared with the rest of the PMU. Its accuracy is 110 ns., in agreement with the expected one:

$$T_m = T/2 + T_{\text{proc}} \tag{5.1}$$

being T the windows length that, as a recall, is set to 60 ms and T_{proc} the overall processing time (see Section 4.3.2 for further details). Note that T_{proc} is slightly larger than the sum of the synchrophasor computation latencies shown in Table 4.1, in view of the communication delays between the MSDFT and synchrophasor estimation processes.

5.3.4 Measurement Reporting Rates

As demonstrated in Section 4.3 the i-IpDFT-based PMU prototype built on the design proposed in Section 4.3 where the MSDFT technique has been adopted, can achieve reporting rates up to the PMU sampling rate F_s.
A dedicated test was designed to verify the advantages brought by this outstanding characteristic. In particular Figure 5.11 shows the sequence of amplitude estimations produced by

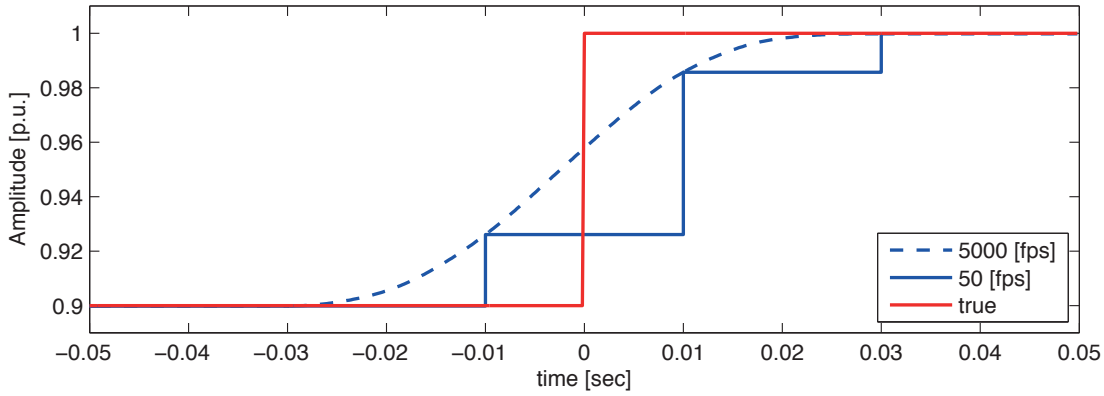


Figure 5.11 – Estimated amplitude profiles during an amplitude step by PMUs characterized by reporting rates of 50 and 5000 [fps] respectively.

the proposed PMU prototype during a step change in the amplitude of the input signal. In particular, Figure 5.11 shows the estimated amplitude during such a sudden change by two different PMUs running the same i-IpDFT algorithm: the only difference is that the first one (blue continuous line) is configured with a reporting rate of 50 frames-per-second, the second one (blue-dashed line) is configure with a reporting rate of 5000 estimated synchrophasors per second. As it can be noticed the second configuration offers a time-resolution proportional to the reporting rate. Obviously, the MSDFT does not affect the PMU response times during the step tests that will maintain the same values demonstrated in Section 5.3.3.

5.3.5 Effectiveness Evaluation of ROCOF Estimator

In order to prove the effectiveness of the ROCOF estimator proposed in Section 4.4.1, Figure 5.12 shows the comparison between the RFE of the above-mentioned estimator and an estimator based on the finite difference formula expressed by equation (4.8) only. In order to demonstrate its efficiency during both static and dynamic conditions, the comparison is performed using different input signals: single-tone and amplitude step tests.
In particular, the upper graph of Figure 5.12 compares the two estimators when the PMU inputs are fed with a single-tone signal characterized by a nominal frequency of 50 Hz. During this test it is evident that the proposed ROCOF estimator never leaves its state S1 (Static conditions) and that the low-pas filter, when activated, improves significantly the ROCOF accuracy in static conditions. On the other hand the estimator based on equation (4.8) is not compliant with the IEEE Std. limits.
The lower graph compares the two estimator during a step change in the synchrophasor amplitude. As it can be noticed, before and after the step the proposed estimator outperforms the simple one described by equation (4.8) as it detects static conditions (state S1) and activates the low-pass filter. On the other hand, during the step change, the estimator identifies a sudden change in the estimated synchrophasor, changes its state in S2 (Dynamic conditions)

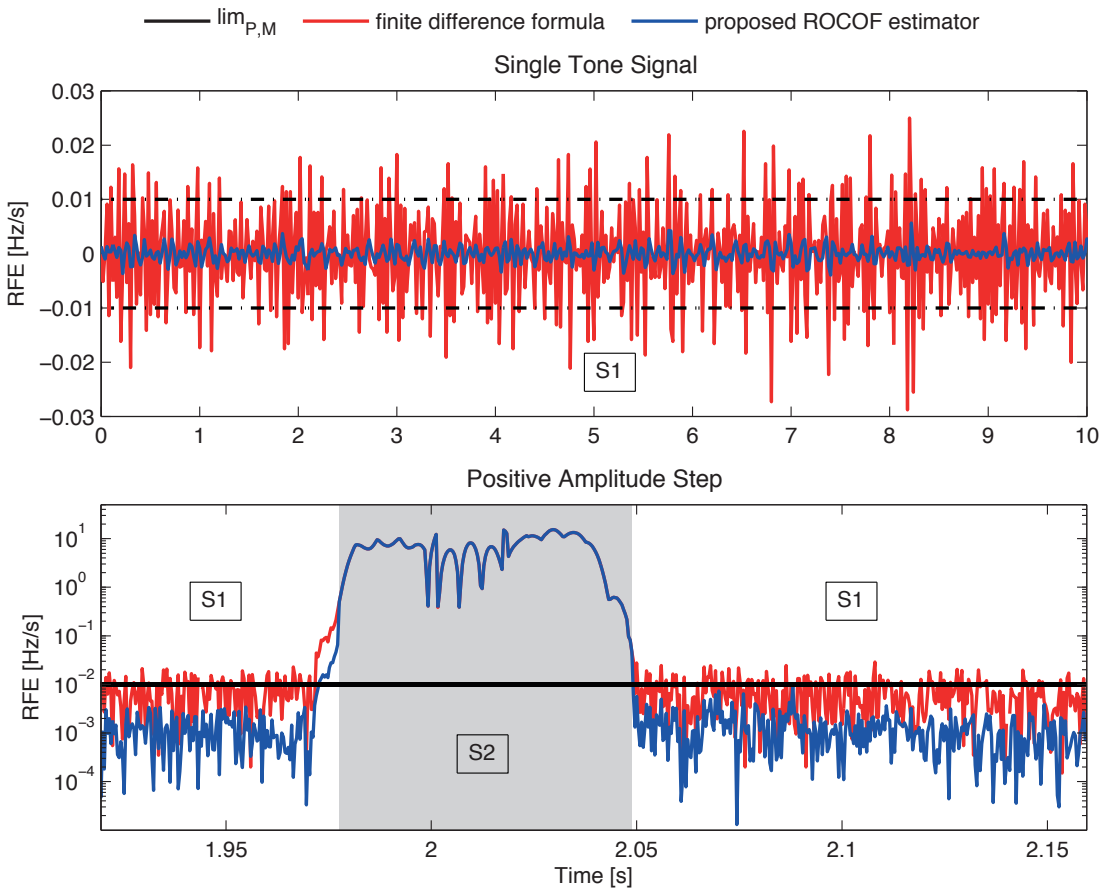


Figure 5.12 – Comparison between the proposed ROCOF estimator and a classical finite difference formula for the approximation of the first-order derivative of frequency.

and deactivates the low-pass filter. As it can be noticed during this period (the gray area in the graph), the proposed ROCOF estimator is superposed to the simple one, allowing the fastest possible recovery to normal operating conditions.

5.4 Experimental Verification of the ADN Compliance

The same setup adopted in the previous Section to verify the PMU compliance to the IEEE Std. C37.118 [1] has been used to test and metrologically characterize the PMU performances during operating conditions not accounted by the IEEE Std C37.118 [1] and representing typical operating conditions of ADNs.
In particular, according to what stated in Chapter 2, three additional test were designed to verify the PMU compliancy with the typical operating conditions of ADNs:

- a test to verify the PMU estimation accuracy with signals corrupted by multiple superposed harmonic components with a fundamental frequency in the range $f_0 \pm 5$

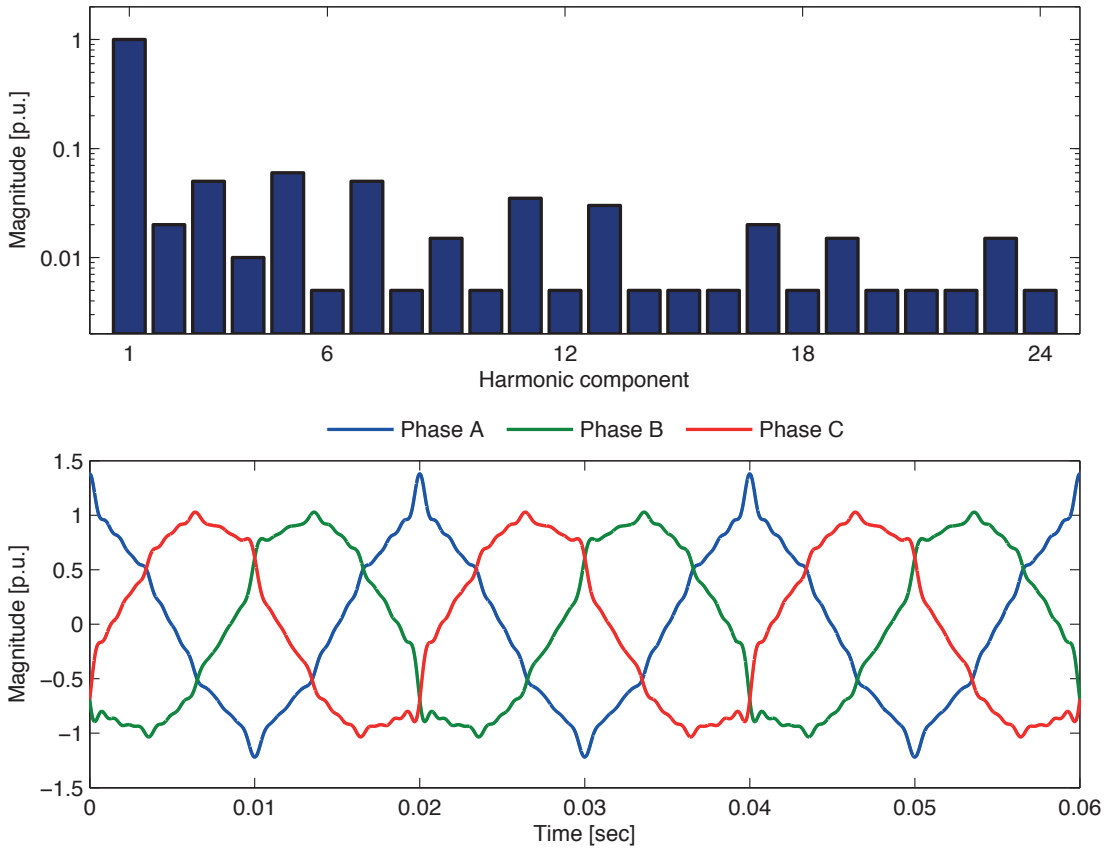


Figure 5.13 – The harmonic content (on top) and associated three-phase waveforms (below) of the reference signal used to verify the PMU robustness to multiple superposing harmonics. The harmonic content correspond to the limits dictated by the European Standard EN50160.

Hz;

- a test to asses the accuracy of the developed PMU prototype when single tone signals are corrupted with typical measurement noise.
- a test to verify the PMU performances during fault events. In this respect a decaying DC offset was used to model this kind of dynamics;

In what follows, the test results are presented in terms of the measured TVE, FE and RFE that are plotted in function of the varied parameters. These error quantities are compared in every graph with the most demanding error limits defined in [1].

5.4.1 Harmonic Interference

As discussed in Section 2.3 the harmonic distortion characterizing voltage and current waveforms of ADNs is significant and might be the source of gross estimation errors if not properly taken into account. Contrary to what reported in the IEEE Std. C37.118 [1], multiple harmonic

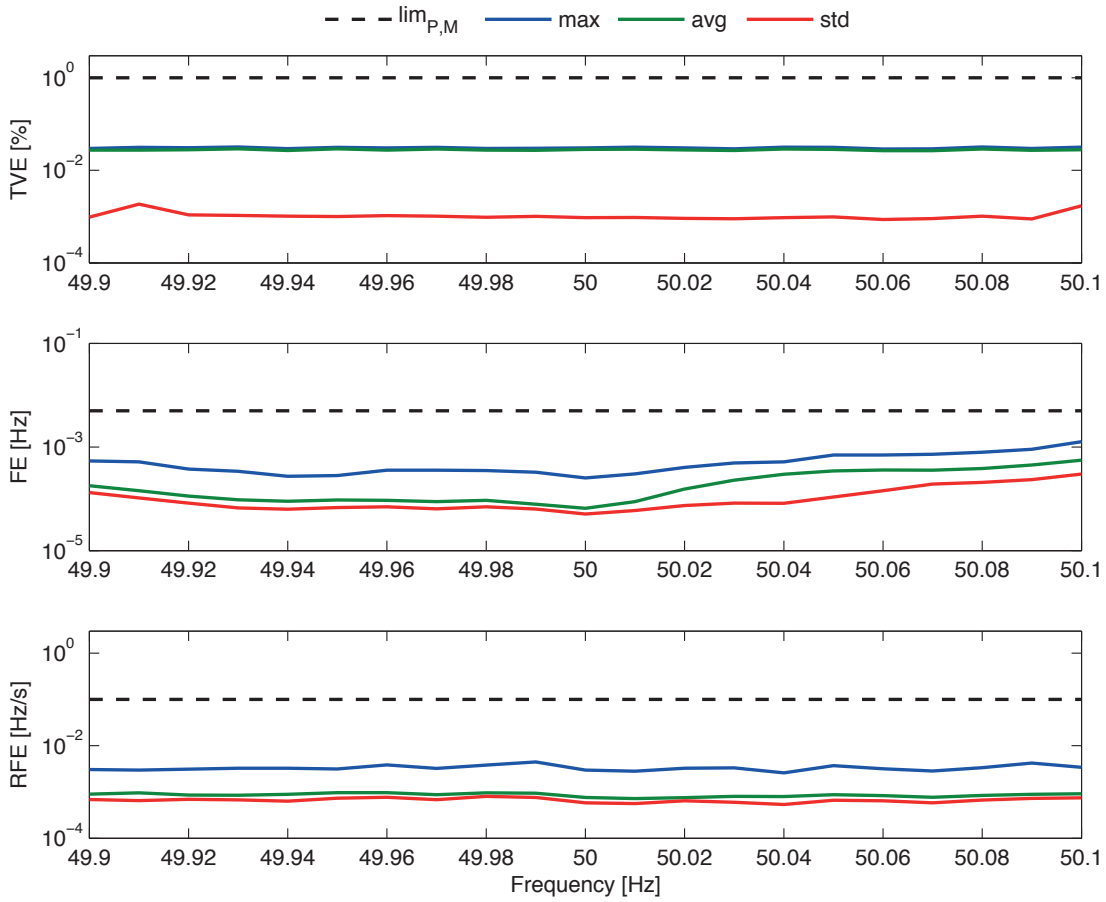


Figure 5.14 – The TVE, FE and RFE as a function of the nominal frequency of a signal corrupted by 23 superposed harmonics characterized by the spectrum presented in Figure 5.13.

components might interfere simultaneously on the tone at the nominal system frequency. Additionally, harmonics of a frequency that does not exactly correspond to the nominal one f_0 must be considered as any power system is rarely operated exactly at 50 or 60 Hz.
In this respect, the limits dictated by the European Standard EN-50160 regarding Voltage characteristics of electricity supplied by public distribution systems [107] were used to synthesize and generate through the developed PMU calibrator an harmonic signal where a steady-state component is corrupted by 23 superposed harmonic for a Total Harmonic Distortion (THD) of approximately 12% (see Figure 5.13). In order to further stress the PMU performances, the nominal frequency has been varied between each sub-test by step of 0.01 Hz in the range between 49.9 and 50.1 Hz to emulate the fact that the power system is rarely operated at its nominal frequency f_0.
The experimental results show the maximum, average and standard deviation values of TVE, FE and RFE as a function of the nominal frequency of the reference signal (see Figure 5.14). As it can be noticed by comparing these results with those of Figures 5.6a and 5.6b, the error levels do not change much from those achieved by applying single and multi-tone signals according

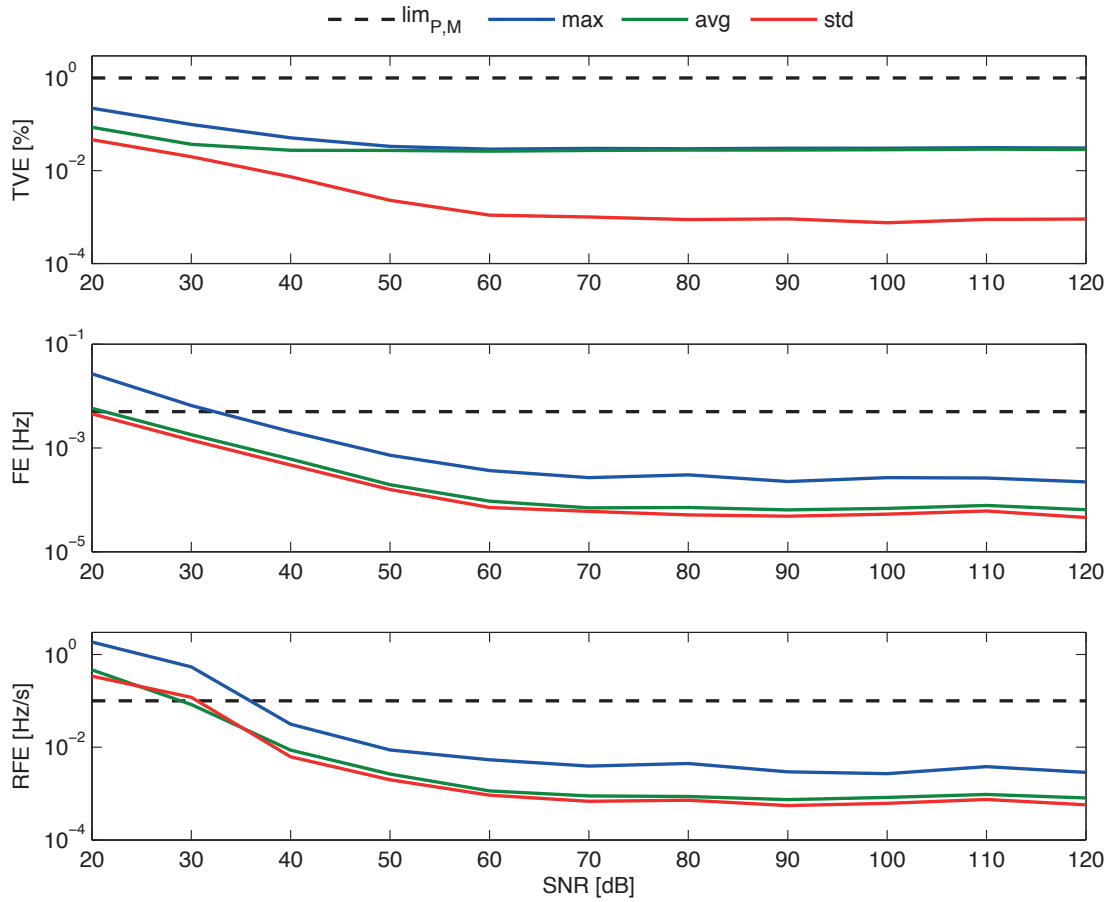


Figure 5.15 – The TVE, FE and RFE as a function of the level of measurement noise present in the input signal. SNRs between 20 and 120 dB have been tested.

to the IEEE Std. [1] testing conditions. The PMU has demonstrated to be characterized by an uncertainty that is therefore independent from the harmonic distortion levels contained in the input signal.

5.4.2 Wideband Noise

In order to verify the PMU performances in presence of various level of measurement noise the PMU accuracy was evaluated when an ideal 50 Hz signal is corrupted with an Additive White Gaussian Noise (AWGN). In this respect, the PMU calibrator has been configured to synthesize an ideal 50 Hz signal characterized by a certain Signal-to-Noise Ratio (SNR). This quantity, as known, is a measure that compares the level of a desired signal to the level of background noise and is typically expressed in decibel (dB):

$$SNR_{dB} = 10\log_{10}(SNR) = 10\log_{10}\left(\frac{P_s}{P_n}\right) = 10\log_{10}\left(\frac{\sigma_s^2}{\sigma_n^2}\right) \tag{5.2}$$

being P_s and P_n the average power of the signals and background noise respectively, and σ_s and σ_n their characteristic standard deviations.
The additive noise has been generated with a built-in software AWGN function generator embedded in the PXI-based calibrator that takes as input the desired standard deviation σ_n of the background noise. This, has been calculated from the desired SNR as follows:

$$\sigma_n = \sqrt{\frac{\sigma_s^2}{SNR}} = \sqrt{\frac{\sigma_s^2}{10^{SNR_{dB}/20}}} = \sqrt{\frac{RMS_s^2}{10^{SNR_{dB}/20}}} \tag{5.3}$$

being RMS_s the Root Mean Square of the signal. It is worth pointing out that the last equality is valid only for purely AC signals, namely for signals characterized by a 0 mean.
The PMU has then been fed with signal characterized by increasing values of SNR between 20 and 120 dB. The maximum, average and standard deviation values of the TVE, FE and RFE are shown in Figure 5.15 as a function of the SNR. As it can be noticed, the PMU performances are worsening and exceeding the IEEE Std. limits from values of SNR higher than 35 dB for both FE and RFE but always stay within the allowable TVE limits. Nevertheless it should be considered that values of SNR lower than 40 dB are quite rare in ADNs and are typically related to incorrectly designed substation installations. As a consequence we can conclude that the PMU is quite robust to the interference produced by the measurement noise. As already discussed in Chapter 3, this is mainly related to the fact that, by adopting a relatively high sampling rate, the effects of noise are considerably reduced.

5.4.3 Decaying DC Offset

A further test has been implemented to evaluate the PMU performances when a decaying DC offset is superposed to a single-tone signal at the rated frequency of the system f_0:

$$s(t) = A\cos(2\pi f_0 t) + A_{\mathrm{DC}} \cdot e^{-t/\tau} \tag{5.4}$$

where the decaying DC offset is modeled in terms of its time constant τ and its initial value A_{DC}.
The values of these parameters have been selected in order to represent typical waveforms of short-circuit currents taking place in a power grid. In particular, Figure 5.16 shows the maximum TVE, FE and RFE when applying a decaying DC offset characterized by an initial value A_{DC} equal to 70% of the nominal magnitude of the single-tone signal and a time constant τ in the range between 0.1 and 10 seconds.
As it can be noticed, the PMU performances deteriorate as the value of time constant τ becomes smaller (i.e., the dynamic becomes faster). This is expected, since in such a condition the signal cannot be anymore considered stationary within the time window T. In general, by comparing the PMU errors with the IEEE Std. limits for single-tone signals (see Figure 5.16), it can be noticed that for $\tau > 0.7$ [sec], the PMU performances are within the IEEE Std. limits and can be compared to those characterizing single-tone signal test.

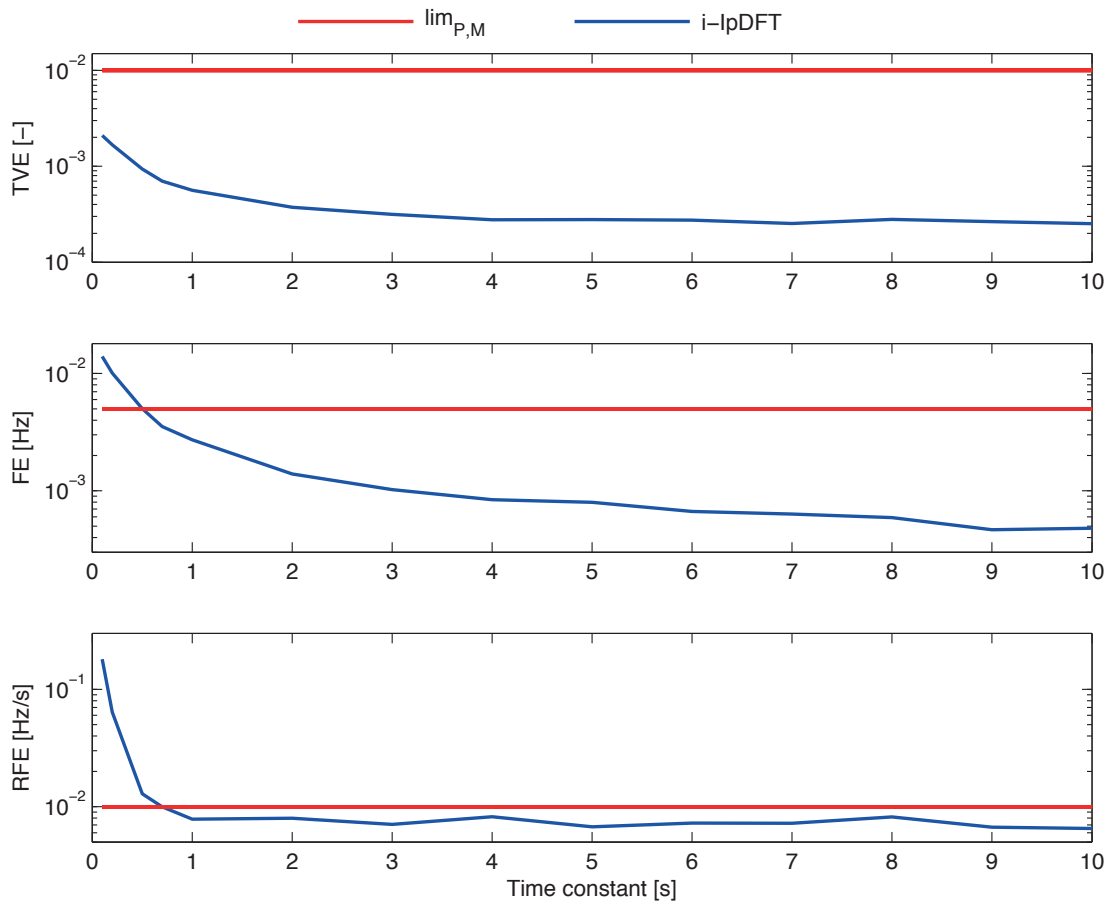


Figure 5.16 – The TVE, FE and RFE as a function of the time constant of a decaying DC offset superposed to a steady-state signal at nominal.

Conclusions

This thesis has proposed a novel methodology in the field of synchrophasor estimation and presented its integration in a PMU prototype that has demonstrated to be compatible with ADN operating condition requirements. In particular the thesis has illustrated and discussed every single stage needed to develop a Phasor Measurement Unit, starting from the definition of the PMU accuracy requirements, to the experimental verification of the performances of the developed PMU prototype.

The PMU design has started from the definition of the measurement accuracies that are needed to correctly operate in ADNs. In particular, the requirements have been derived for the most common PMU application, i.e., power-system monitoring, using the results of dedicated simulations aimed at replicating typical operating conditions of ADNs. The analysis has demonstrated that PMUs expected to operate in ADNs must be characterized by TVE values that are at least two order of magnitude below the 1% TVE limit specified in the IEEE. Std. C37.118. Even though such a result was partially expected, as [1] was originally conceived for PMU applications in transmission networks, the proposed analysis has the merit to have quantified these differences. In particular, the PMU requirements have demonstrated to be more demanding for voltage phasors rather than current phasors, when using PMUs to monitor ADNs characterized by nominal voltages higher then 20 kV. On the other hand, the voltage phasor accuracy requirements soften when using PMUs to monitor ADNs characterized lower nominal voltages (e.g., 4.16 kV), whereas the current phasor accuracy requirements become tighter.

Based on the accuracy requirements derived in Chapter 2, a novel SE algorithm, called iterative-Interpolated DFT (i-IpDFT), has been developed. The proposed SE algorithm represents an extension of the classical IpDFT approach as it includes a scheme for the compensation of the effects of the self-interaction between the positive and the negative image of the spectrum. This modification has been conceived to improve the PMU performances during both static and dynamic conditions and, at the same time, allow a feasible deployment of the algorithm into an FPGA-based PMU prototype. The formulation of such a technique has started from the observation that the spectral leakage is the most relevant source of errors when using the DFT to estimate the parameters of a sinusoidal signal. This is even more evident in applications like synchrophasor estimation that usually adopt relatively short windows to reduce the PMU measurement reporting latencies and response times. Nevertheless, through computer simulations, it has been demonstrated that the i-IpDFT technique outperform classical IpDFT

methods, also by adopting shorter windows that are usually worsening the estimation uncertainty of any SE algorithm. In particular, the effects of the proposed iterative compensation of the negative spectrum image are visible up to the 4^{th} iteration. Furthermore, we have verified that, by adopting the i-IpDFT technique, the synchrophasor estimation accuracy is not affected by the instantaneous frequency of the power system and is characterized by a uncommonly flat frequency response.
The proposed i-IpDFT SE algorithm has also demonstrated to be characterized by a relatively low computational complexity compared to other SE techniques. This is a non negligible advantage when integrating the proposed technique into a PMU prototype that could exploit the availability of relatively cheap embedded systems. In this respect the thesis has illustrated the development of a PMU prototype based on an FPGA hardware platform and discussed the non-trivial aspects related to the optimal deployment of the proposed SE algorithm on the FPGA platform. In order to increase the SE algorithm throughput, the proposed i-IpDFT technique has been coupled with the MSDFT, an efficient and stable sample-by-sample DFT update method that is capable of accelerating the reporting rates of any DFT-based synchrophasor estimation algorithm up to a limit corresponding to the PMU sampling rate.
Additionally, the synchronization of the developed SE process to the UTC-time reference provided by a GPS receiver has been discussed and two different techniques aimed at compensating the characteristic drift of a free-running oscillator have been presented. The first refers to the real-time measurement and compensation of the drift itself and has demonstrated to considerably improve the PMU frequency estimations. The second refers to the compensation of the time difference between the UTC-PPS rising edge and the first sample of the window and has demonstrated to improve the PMU phase estimations up to a value corresponding to the characteristic sample time of the PMU.
Finally the developed PMU prototype has been metrologically characterized using a PMU calibrator developed in collaboration with the Swiss Federal Institute of Metrology (METAS). The proposed calibrator has demonstrated to be characterized by an uncertainty that is much lower than the on of most of the available PMU calibration platforms available nowadays, including the one developed by NIST that is widely recognized as the reference one.
The calibration results have verified the PMU compliancy with the P-class requirements defined in IEEE Std. C37.118 and with most of the accuracy requirements defined for M-class PMUs with the exception of OOB interference tests. The calibration results have also compared the performances of the proposed i-IpDFT SE technique characterized by a single iteration to compensate the effects of the spectral interference, with a standard IpDFT method characterized by the same window length (3-periods) and window type (Hanning). This verification has further quantified the effects of the iterative compensation also when deployed in a real PMU prototype. In particular the developed PMU, is characterized by a steady state TVE of 0.02% that is independent of the instantaneous frequency of the power system and is also maintained with superposed harmonics of any order and during frequency sweeps. The PMU performances are slightly worse during amplitude and phase modulations but still within the IEEE Std. limits. The response times are as well within the limits and always lower than 28 ms for TVE, 30 ms for FE and 70 ms for RFE. Furthermore, the developed prototype is

characterized by an extremely deterministic an reduced measurement reporting latency that is slightly higher than 30 ms and by measurement reporting rates that are only limited by the PMU sampling rate (nevertheless, using reporting rates higher than 200-240 fps is strongly discouraged).
The developed PMU prototype has also been tested against typical operating conditions of ADNs. In this respect three additional tests have been designed: (i) a test to verify the PMU accuracy when analyzing a signal characterized by 23 harmonics (total THD of approximately 12%) superposed to a main tone at a frequency that has been varied in the range $[49.9, 50.1]$ Hz; (ii) a test designed to verify the PMU performances when a single tone signal is corrupted with wideband noise (in particular, SNR between 20 and 120 dB have been tested); (iii) a test to verify the deterioration of the PMU accuracy with signals composed by a main tone superposed to a decaying DC offset characterized by smaller time constants in the range $[0.1, 10]$ seconds. The developed PMU has demonstrated to be robust to any of the considered operating conditions and its accuracy deteriorates only for values of SNR lower than 35 dB and time constants of the decaying DC offset lower than 0.5 seconds.
It is also worth mentioning that the developed PMU prototype has been recently adopted by three European utilities to compose the backbone of a distributed monitoring infrastructure for three different ADNs. In particular the following electrical grids are currently operated using the PMU prototype presented in this thesis:

- a 18 buses MV (10 kV) grid, operated by the Dutch DNO Alliander and feeding the city of Huissen, the Netherlands, that has been equipped with 10 PMUs reporting data 50 times per second to a PDC located 100 kilometers away through a public 4G connection;
- the EPFL campus MV grid (20 kV), operated by the Swiss DNO Romande Energie, and composed by 40 buses (i.e., equivalent to the size of a city of about 20'000 inhabitants) that will be soon fully equipped with PMUs in every node (real-time measurements are available online [108]);
- the sub-transmission network (125 kV) of the city of Lausanne, Switzerland, where 15 PMUs have been deployed by the local system operator (Services Industriels de Lausanne – SiL) to monitor current flows and nodal voltages in everyone of the 7 buses of the system.

We can therefore conclude that the proposed SE algorithm and associated PMU prototype exhibits peculiar characteristics that enable its use in ADNs.

A Appendix

A.1 The Fourier Transform of the Rectangular Window

The rectangular window is defined as:

$$w_r(t) = \begin{cases} 1, & \text{if} \quad -\frac{T}{2} \leq t < \frac{T}{2} \\ 0, & \text{otherwise} \end{cases} \tag{A.1}$$

being $T = N/F_s$ the window length. Its Fourier transform can be computed as follows:

$$w_r(t) \xrightarrow{\mathfrak{F}} W_r(f) = \int_{-\infty}^{+\infty} w(t) \cdot e^{-j2\pi ft} \mathrm{d}t \tag{A.2}$$

$$= \int_{-\frac{T}{2}}^{+\frac{T}{2}} 1 \cdot e^{-j2\pi ft} \mathrm{d}t \tag{A.3}$$

$$= \frac{1}{-j2\pi f} \left[e^{-j2\pi ft} \right]_{-\frac{T}{2}}^{+\frac{T}{2}} \tag{A.4}$$

$$= \frac{1}{-j2\pi f} \left[e^{-j\pi fT} - e^{j\pi fT} \right] \tag{A.5}$$

$$= \frac{1}{-j2\pi f} \left[e^{-j\pi fT} - e^{j\pi fT} \right] \tag{A.6}$$

$$= \frac{1}{-j2\pi f} \left[-2j \sin(\pi fT) \right] \tag{A.7}$$

$$= T \frac{\sin(\pi fT)}{\pi fT} \tag{A.8}$$

$$\triangleq T \operatorname{sinc}(fT) \tag{A.9}$$

As shown in Figure A.1, the sinc function has a decaying profile with zero crossings that are equally spaced in the x-axis and happens at integer multiples of $1/T$, being T the rectangular window width.

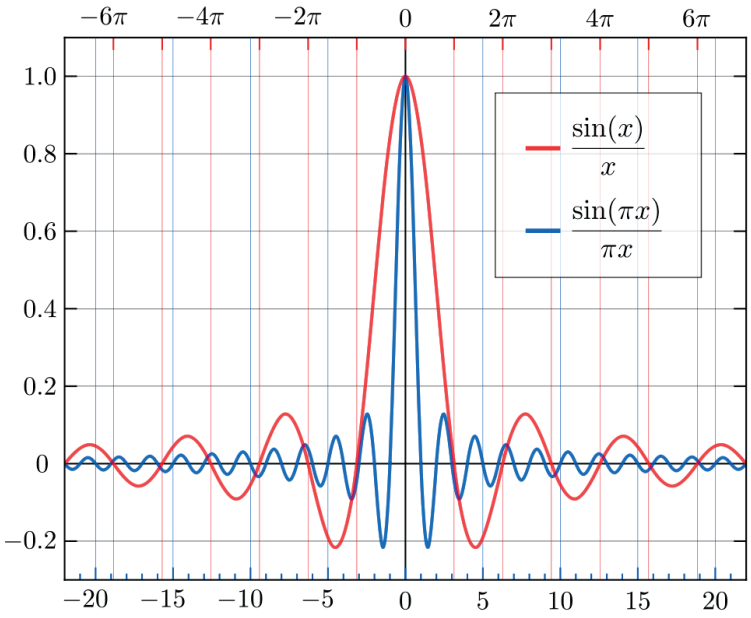


Figure A.1 – The sinc function.

A.2 Approximation of the Spectrum of the Hanning Window

As known, the Fourier Transform of the discrete-time Hanning Window can be expressed as a linear combination of three Dirichlet kernels opportunely shifted in frequency:

$$
\begin{aligned}
W_H(\omega) &= -0.25 \cdot W_R(\omega - 2\pi/N) + 0.5 \cdot W_R(\omega) - 0.25 \cdot W_R(\omega + 2\pi/N) \\
&= -0.25 \cdot e^{-j\omega(N-1)/2} \cdot e^{j\pi(N-1)/N} \cdot \frac{\sin(\omega N/2 - \pi)}{\sin(\omega/2 - \pi/N)} + \\
&\quad + 0.5 \cdot e^{-j\omega(N-1)/2} \cdot \frac{\sin(\omega N/2)}{\sin(\omega/2)} + \\
&\quad - 0.25 \cdot e^{-j\omega(N-1)/2} \cdot e^{-j\pi(N-1)/N} \cdot \frac{\sin(\omega N/2 + \pi)}{\sin(\omega/2 + \pi/N)} \\
&\approx -0.25 \cdot e^{-j\omega(N-1)/2} \cdot (-1 + j\pi/N) \cdot \frac{-\sin(\omega N/2)}{\sin(\omega/2 - \pi/N)} + \\
&\quad + 0.5 \cdot e^{-j\omega(N-1)/2} \cdot \frac{\sin(\omega N/2)}{\sin(\omega/2)} + \\
&\quad - 0.25 \cdot e^{-j\omega(N-1)/2} \cdot (-1 - j\pi/N) \cdot \frac{-\sin(\omega N/2)}{\sin(\omega/2 + \pi/N)} \\
&\approx -0.25 \cdot e^{-j\omega(N-1)/2} \cdot \frac{\sin(\omega N/2)}{\sin(\omega/2 - \pi/N)} + \\
&\quad + 0.5 \cdot e^{-j\omega(N-1)/2} \cdot \frac{\sin(\omega N/2)}{\sin(\omega/2)} + \\
&\quad - 0.25 \cdot e^{-j\omega(N-1)/2} \cdot \frac{\sin(\omega N/2)}{\sin(\omega/2 + \pi/N)}
\end{aligned}
\tag{A.10}
$$

where the approximation $e^{\pm j\pi(N-1/N)} \approx -1 \pm j\pi/N$ was used. This only holds if $N \gg 0$.

A.3 DFT Modulation Property

Thesis:
If

$$x(n) \Longleftrightarrow X_k$$

then

$$W_N^{mn} \cdot x(n) \Longleftrightarrow X_{k-m}$$

Proof:

$$\begin{aligned} g(n) := W_N^{mn} \cdot x(n) \Longleftrightarrow G_k &= \sum_{n=0}^{N-1} g(n) \cdot W_N^{-kn} \\ &= \sum_{n=0}^{N-1} W_N^{mn} \cdot x(n) \cdot W_N^{-kn} \\ &= \sum_{n=0}^{N-1} x(n) \cdot W_N^{-(k-m)n} \\ &= X_{k-m} \end{aligned}$$

A.4 On the Correct Numerical Representation of the MSDFT

Let's consider a signal $x(n) = 0$ for $n = 0$ and, as en example, $M = 4$ and . From equation (3.39) we have the following:

$$
\begin{aligned}
n = 0: \quad & X_0(0) = x(0) \\
n = 1: \quad & X_0(1) = [x(0)] + x(1) \cdot W_4^{-k} \\
n = 2: \quad & X_0(2) = \left[x(0) + x(1) \cdot W_4^{-k} \right] + x(2) \cdot W_4^{-2k} \\
n = 3: \quad & X_0(3) = \left[x(0) + x(1) \cdot W_4^{-k} + x(2) \cdot W_4^{-2k} \right] + x(3) \cdot W_4^{-3k} \\
n = 4: \quad & X_0(4) = \left[\cancel{x(0)} + x(1) \cdot W_4^{-k} + x(2) \cdot W_4^{-2k} + x(3) \cdot W_4^{-3k} \right] - \cancel{x(0)} + x(4) \\
n = 5: \quad & X_0(5) = \left[\cancel{x(1) \cdot W_4^{-k}} + x(2) \cdot W_4^{-2k} + x(3) \cdot W_4^{-3k} + x(4) \right] - \cancel{x(1) \cdot W_4^{-k}} + x(5) \cdot W_4^{-k} \\
n = 6: \quad & X_0(6) = \ldots
\end{aligned}
$$

where the expressions between brackets come from the previous iteration.

Any mSDFT implementation will not be affect by any accumulated error only if at time:

$$\left[x(n-M) \cdot W_M^{-km} \right]_n \equiv \left[x(n) \cdot W_M^{-km} \right]_{n-M}$$

This holds only if a integer/fixed-point numerical representation is used.

List of Acronyms

AC	Alternating Current
ADC	Analog to Digital (A/D) Converter
ADN	Active Distribution Network
ASIC	Application-Specific Integrated Circuit
AWGN	Additive Gaussian Noise
CAPEX	CAPital EXpenditure
cRIO	Compact Reconfigurable I/O (compactRIO)
CT	Current Transformer
DAC	Digital to Analog Converter
DC	Direct Current
DER	Distributed Energy Resource
DFS	Discrete Fourier Series
DFT	Discrete Fourier Transform
DMA	Direct Memory Access
DN	Distribution Network
DNO	Distribution Network Operator
DSO	Distribution System Operator
DSP	Digital Signal Processing
DTFT	Discrete Time Fourier Transform
EMS	Energy Management System
FACTS	Flexible AC Transmission System
FE	Frequency Error
FFT	Fast Fourier Transform
FIFO	First In First Out
FPGA	Field Programmable Gate Array
GLONASS	GLObal NAvigation Satellite System
GNSS	Global Navigation Satellite System
GPP	General Purpose Processor
GPS	Global Positioning System
GPU	Graphical Processing Unit
HTML	HyperText Markup Language
HVDC	High-voltage Direct Current

IED	Intelligent Electronic Device
IEEE	Institute of Electrical and Electronics Engineers
IIR	Infinite Impulse Response
IpDFT	Interpolated Discrete Fourier Transform
IRIG	Inter-Range Instrumentation Group
JSON	JavaScript Object Notation
LPF	Low Pass Filter
LUT	Look-up Table
MAC	Multiply and Accumulate
MASER	Microwave Amplification by Stimulated Emission of Radiation
ME	Magnitude Error
MEO	Medium Earth Orbit
METAS	Swiss Federal Institute of Metrolgy
MSDFT	Modulated Sliding Discrete Fourier Transform
MV	Medium Voltage
NASPI	North American Synchrophasor Initiative
NI	National Instruments
NIST	National Institute of Standards and Technology
NTP	Network Time Protocol
OCXO	Oven-Controlled Crystal Oscillator
OOB	Out-Of-Band
PDC	Phasor Data Concentrator
PE	Phase Error
PID	Proportional Integral Derivative
PMU	Phasor Measurement Unit
PPS	Pulse Per Second
PTP	Precise Time Protocol
PXI	PCI eXtensions for Instrumentation
RAM	Random Access Memory
RER	Renewable Energy Resource
RFE	Rate of change of Frequency Error
RL	Reporting Latency
RMS	Root Mean Square
ROCOF	Rate Of Change Of Frequency
RT	Response Time
RTOS	Real-time Operating System
RTU	Remote termianl Unit
RVCI	Rife Vincent Class I
SAR	Successive Approximation Register
SDFT	Sliding Discrete Fourier Transform
SE	Synchrophasor Estimation
SNR	Signal to Noise Ratio

SoC	System on Chip
STFT	Short-time Fourier Transform
TCP	Transmission Control Protocol
TCXO	Temperature Compensated Crystal Oscillator
TFT	Taylor Fourier Transform
THD	Total Harmonic Distortion
TNO	Transmission Network Operator
TSO	Transmission System Operator
TVD	Total Vector Difference
TVE	Total Vector Error
UDP	User Datagram Protocol
UTC	Coordinated Universal Time
VT	Voltage Transformer
WLS	Weighted Least Square

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RESEARCH INTERESTS

- Smart grids
- Synchrophasor estimation
- Phasor Measurement Units and their synchronization
- Real-time monitoring, protection and control of Active Distribution Networks

EDUCATION

EPFL – Ècole Polytechnique Fèdèrale de Lausanne December 2011 - Present
PhD in Energy, Distributed Electrical System Laboratory (DESL) *Lausanne, Switzerland*

- Thesis title: "Synchrophasor Estimation Algorithms and their Deployment in Advanced Phasor Measurement Units for the Real-time Monitoring of Active Distribution Networks" (supervisor: Prof. Mario Paolone).

ISICT – Institute of Advanced Studies in ICT September 2008 - March 2011
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UNIGE – University of Genoa September 2008 - March 2011
M.Sc. in Electronic Engineering *Genoa, Italy*

- Thesis title: "Control oriented charge acceptance modeling for lead-acid batteries" (supervisor: Prof. Marco Storace).
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PROFESSIONAL EXPERIENCE

INSIS – S.p.A, Special Systems Engineering April 2011 - November 2011
Trainee *La Spezia, Italy*

- SmartPole project: Development and testing of an innovative system for the automatic measurement of height and temperature of the snowpack.
- AKUA project: design and integration within a CAN network of an embedded device complying with CiA 443 profile for subsea systems.

FFA – Ford Forschungszentrum Aachen GmbH June 2010 - December 2010
Intern *Aachen, Germany*

· Development of a control-oriented model and an estimator of the charge acceptance for a lead-acid battery. Planning and execution of tests on lead-acid batteries.
· Industrial case study of MOBY-DIC European project (`http://www.mobydic-project.eu/`).

SCIENTIFIC PUBLICATIONS

Book Chapters

1. "Advances in Power System Modelling, Control and Stability Analysis", by F. Milano, Chapter 3: "DFT-based synchrophasor estimation processes for Phasor Measurement Units applications: algorithms definition and performance analysis", Institute of Engineering and Technology - IET (in preparation).

Journal papers[1]

2. Romano, P.; Paolone, M., "Enhanced Interpolated-DFT for Synchrophasor Estimation in FPGAs: Theory, Implementation, and Validation of a PMU Prototype," IEEE Transaction on Instrumentation and Measurement, vol. 63, no.12, pp. 2824, 2836, Dec. 2014.

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4. Pignati, M; Zanni, L.; Romano, P; Cherkaoui, R.; Paolone, M., "Fault Detection and Faulted Line Identification in Active Distribution Networks using Synchrophasors-based Real-Time State Estimation", submitted to *IEEE Transaction on Power Delivery* (under review).

Conference papers[1]

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10. Hoefling, M.; Heimgaertner, F.; Menth, M.; Katsaros, K.V.; Romano, P.; Zanni, L.; Kamel, G., "Enabling resilient smart grid communication over the information-centric C-DAX middleware,"

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12. Colangelo, D.; Zanni, L.; Pignati, M.; Romano, P.; Paolone, M.; Braun, J.-P.; Bernier, L.-G., "Architecture and characterization of a calibrator for PMUs operating in power distribution systems," in PowerTech, 2015 IEEE Eindhoven, pp.1-6, June 29th-July 2nd 2015

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INVITED TALKS

1. Romano, P.; Paolone, M.,"On the use of Phasor Measurement Units for the Real-Time monitoring of Active Distribution Networks", Electricité de France S.A. (EDF), Paris, France, January 10th, 2014.

2. Romano, P.; Paolone, M., "Advanced PMUs for Active Distribution Networks Based on the e-IpMSDFT Method", Workshop on synchrophasor estimation processes for Phasor Measurement Units: algorithms and metrological characterization, Lausanne, Switzerland, December 9th, 2015.

3. Strobbe, M.; Develder, C.; Paolone, M.; Romano, P.; Pignati, M.; Sarri, S.; Wei Koong Chai; Katsaros, K.V.; Ning Wang; Hoefling, M.; Menth, M.; Bontius, H.; Poll, E.; Adolph, J., "Information-centric communication infrastructure for real-time state estimation of active distribution networks using synchrophasor measurements", NASPI – North American Synchrophasor Initiative Working Group Meeting, San Francisco, USA, March 23rd-24th, 2015.

4. Romano, P.; Kruimer, B.; Paolone, M.,"Real-time Monitoring of the EPFL Campus Distribution Network Using PMUs", i-PCGRID – Innovations in Protection & Control for Greater Reliability Infrastructure Development Workshop, San Francisco, USA, March 25th-27th, 2015.

5. Romano, P.; Pignati, M.; Paolone, M, "Integration of an IEEE Std. C37.118 compliant PMU into the OPAL-RT real-time simulation", RT15 Conference – Opal-RT European User Group Event, Barcelona, Spain, May 27th-28th, 2015.

6. Romano, P.; Paolone, M., "Real-time Monitoring of Active Distribution Networks Using PMUs: Requirements and Real Test Cases", NASPI – North American Synchrophasor Initiative Working Group Meeting, Chicago, USA, October 14th-15th, 2015.

RESEARCH PROJECTS

C-DAX October 2012 - March 2016

· Cyber-secure Data And Control Cloud for future power distribution networks (`http://www.cdax.eu`).
· Experimental validation with a real PMU deployment in a medium voltage grid in Huissen, the Netherlands, operated by Alliander.

NanoTera SmartGrid April 2013 - April 2017

· Smart grids, smart buildings and smart sensors for optimized and secure management of the electricity distribution using dedicated micro-electronic ICS and real-time ICT (`smartgrid.epfl.ch`).
· Development of new technologies dedicated to the real time monitoring and management of smart grids with validation in the EPFL campus.

ENG52 SmartGrid II September 2014 - May 2017

· Measurement tools for Smart Grid stability and quality (`https://www.euramet.org/`).
· Development of new calibration methods and technologies for Phasor Measurement Unit expected to operate in Distribution Networks.

RT-PMU January 2014 - January 2017

· Installation of 15 Phasor Measurement Units in the sub-transmission network operated by Services industriels de Lausanne (SiL).
· Upgrade of the SCADA system of SiL by integrating a real-time state estimation process based on Phasor Measurement Units.

INDUSTRIAL COLLABORATIONS

National Instruments December 2012 - Present

· Development of the class-P software of the Phasor Measurement Unit offered by National Instruments as part of its Grid Automation System.
· Participation to the "NIST assessment of PMU performances" aimed at verifying the IEEE Std. C37.118.1-2011 requirements.
· Participation to a preliminary PMU installation in Western Region, India under a pilot project on WAMS coordinated by POSOCO.

SUPERVISED STUDENTS

- Nicotra D., "Modelli di Reti Elettriche di Distribuzione in Sistemi di Simulazione in Real-time", M.Sc. Thesis project, Spring Semester 2011-2012.
- Pignati, M., "Integration of Phasor Measurement Units in Active Distribution Networks: Real-Time Synchronization and Data Collection", M.Sc. Thesis project, Fall Semester 2012-2013.
- Di Labio, E.,"FPGA Code Optimization For High Accurate Phasor Measurement Units", Semester Project, Fall Semester 2013-2014.
- Di Labio, E.,"Integration of an IEEE Std. C37.118 compliant PMU into the OPAL-RT real-time simulation", M.Sc. Thesis project, Spring Semester 2013-2014.
- Tastemiroglou, K., "Analysis and Development of Enhanced IpDFT Synchrophasor estimation algorithms, capable of meeting IEEE std C37.118 requirements", M.Sc. Thesis project, Spring Semester 2013-2014.
- Varescon, E., "Latency Optimization on LabVIEW", Summer project, 2014.

- Derviskadic, A., "Development of a PMU-based RTSE of subtransmission networks: theory and experimental validation based on the Lausanne 125 kV grid", M.Sc. Thesis project, Spring Semester 2014-2015.

TEACHING EXPERIENCE

- Assistant Lecturer for the "Smart-grid Technologies" course, M.Sc. in Smart Grids Science and Technology, EPFL, 2014-present.

PEER REVIEWS

- IEEE Transactions on Instrumentation and Measurement, since 2014
- Elsevier Mechanical Systems and Signal Processing, since 2015
- Elsevier Sustainable Energy, Grids and Networks Journal, since 2014
- 19^{th} Power Systems Computation Conference (PSCC), 2016

LANGUAGE SKILLS

Italian	Mother tongue.
English	Full professional proficiency.
French	Full professional proficiency.
German	Elementary understanding of written text and oral communication.